

Compal Confidential

QCL51 Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Chelsea Pro M2

Muxless/UMA / PX 4.0 / PX 5.0

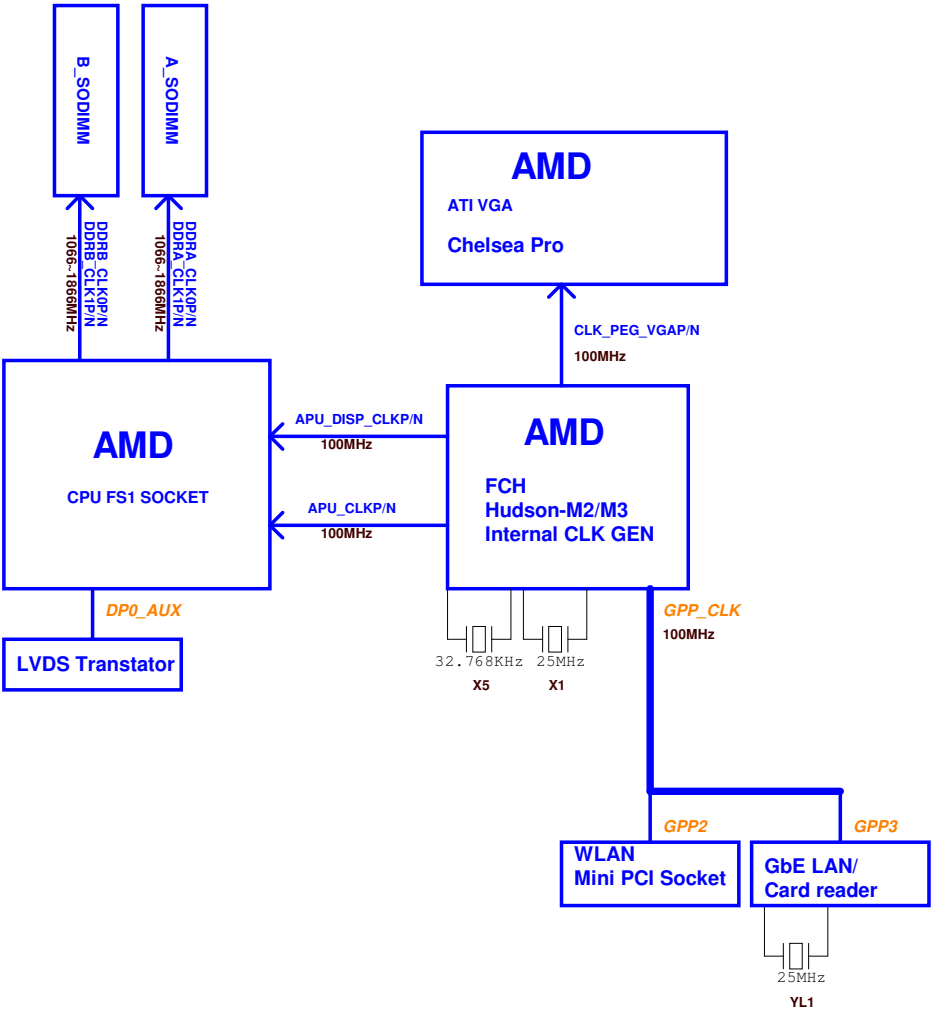
2011-10-26

LA-8712P REV: 0.1

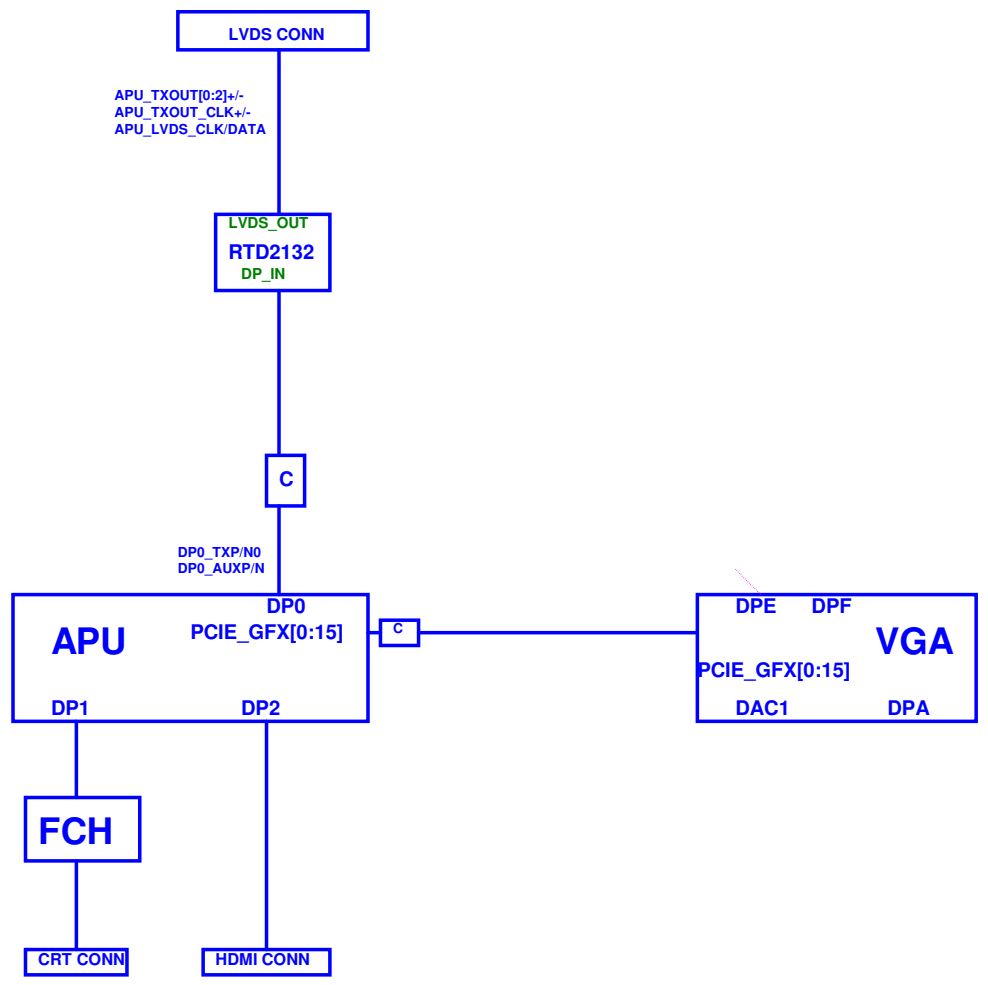
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				QCL51 LA-8712P	0.1
				Date	Monday, November 28, 2011
				Sheet	1 of 56

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	Block Diagrams
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CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rb	100K +/- 5%			
Board ID	Ra / Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

ZZZ1



PCB
Part Number = DA80000SH00
PCB 00H LA-8712P REV0 M/B

BOARD ID Table

Board ID	PCB Revision
0	DB
1	
2	
3	
4	
5	
6	
7	

BOM Option Table

BOM
Structure
PX@

Description
PX function

BOM Config

UMA
PX
V

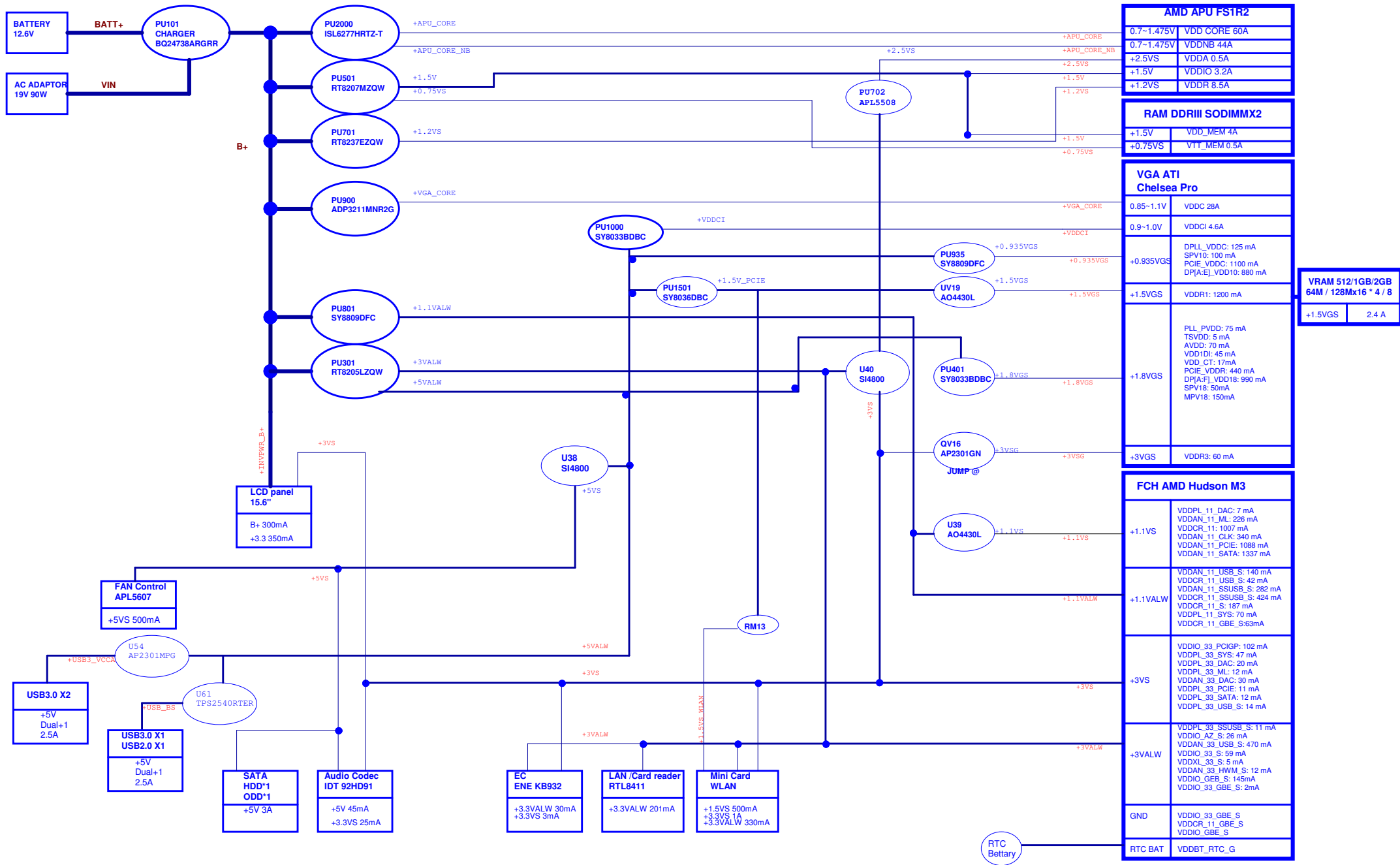
x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices			
Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH (S0) SM Bus 0 address			FCH (S0~S5) SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0	Touch pad		
DDR DIMM2	1010 001X b	A2			
Amplifier					

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13 PCIE_GTX_C_FRX_P[0..15]

13 PCIE_GTX_C_FRX_N[0..15]

PCIE_FTX_C_GRX_P[0..15] 13

PCIE_FTX_C_GRX_N[0..15] 13

GPU

GLAN/Card reader
WLAN

UMI

GPU

GLAN/Card reader
WLAN

UMI

JCPU1A

PCI EXPRESS

GRAPHICS

GPP

UMI

+1.2VS R539 1 2 P_ZVDDP AG11 196_0402_1%

P_ZVDDP W/S=8/12 mil, <3000mil

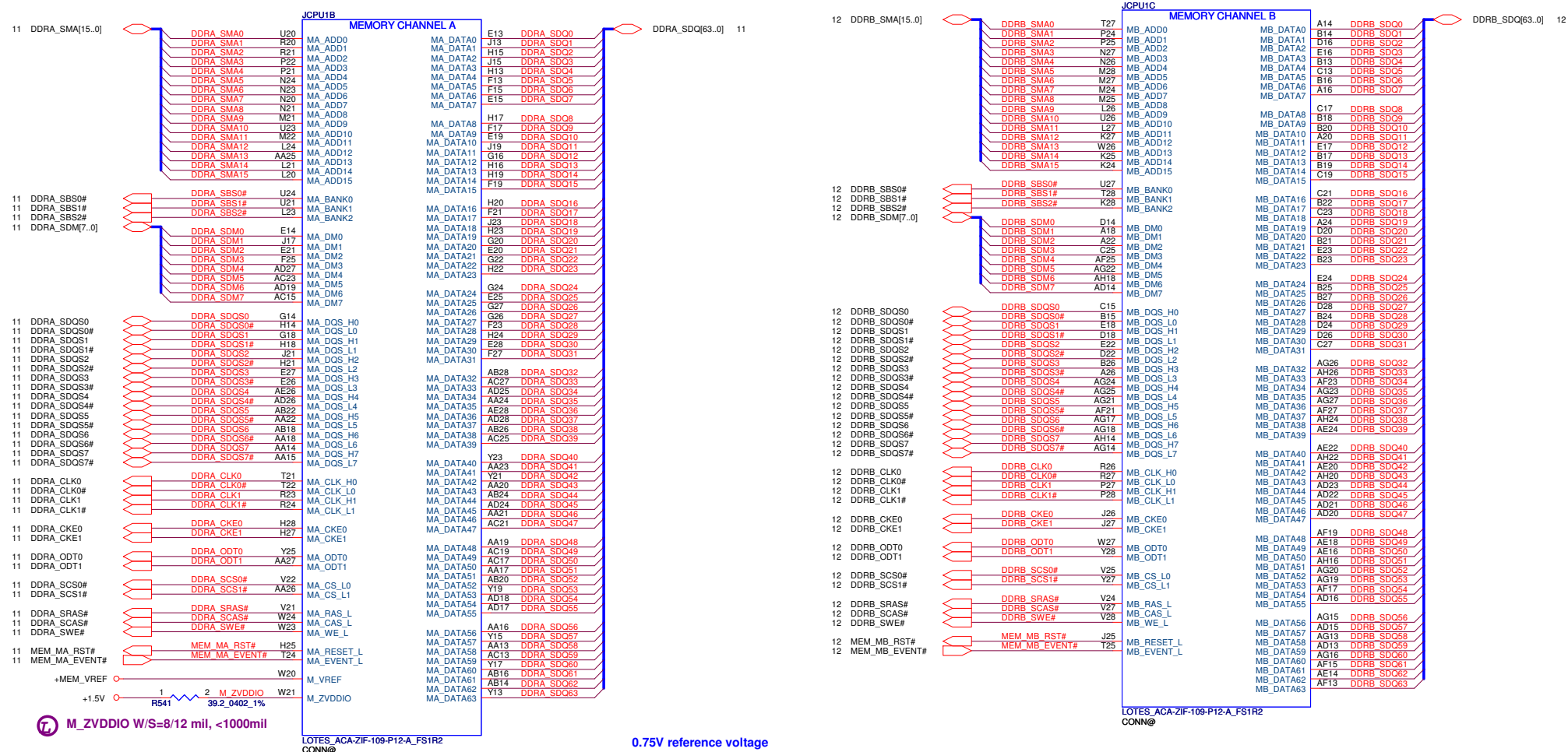
LOTES_ACA-ZIF-109-P12-A_FS1R2
CONN@

P_ZVSS

AH11 P_ZVSS 1 2 R540 196_0402_1%

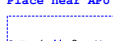
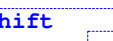
P_ZVSS W/S=8/12 mil, <3000mil

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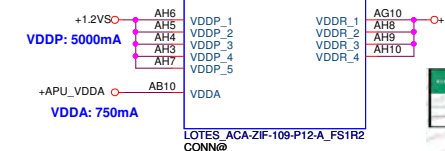
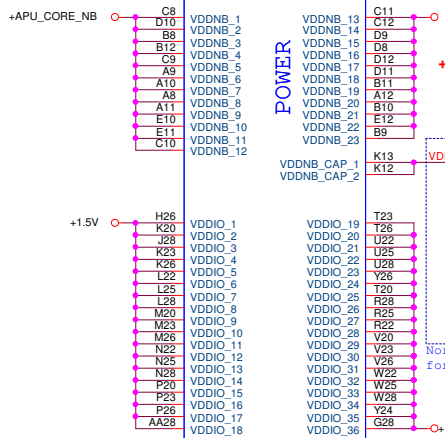
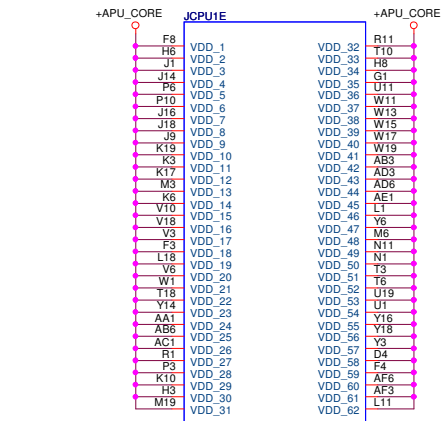
100MHz



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					Customer	
					Date	
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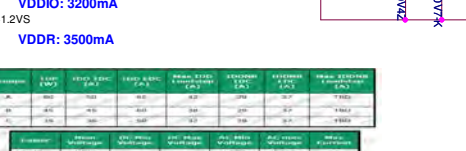
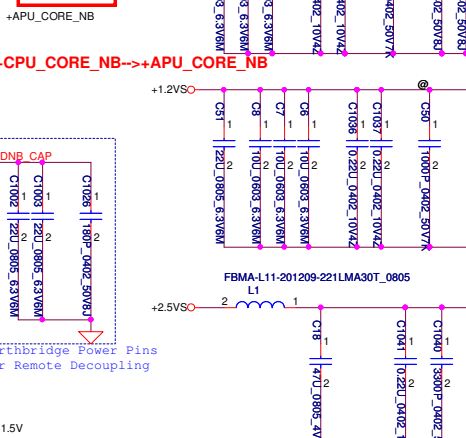
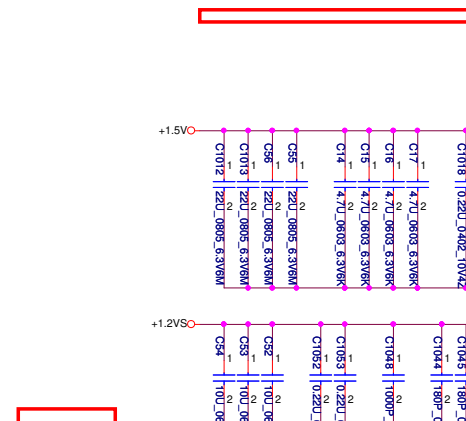
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A

+CPU_CORE-->+APU_CORE



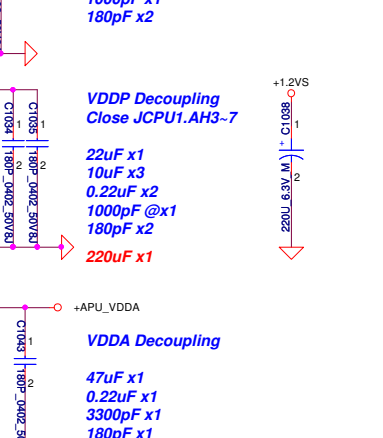
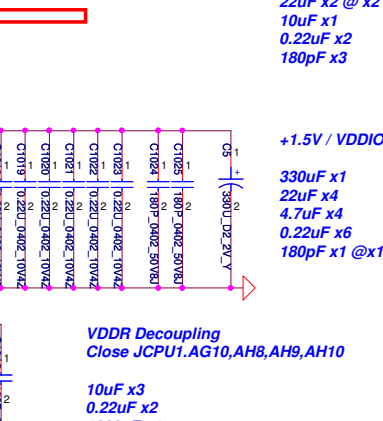
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Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2	
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16	

+CPU_CORE_NB-->+APU_CORE_NB



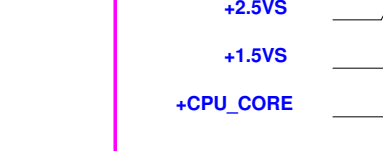
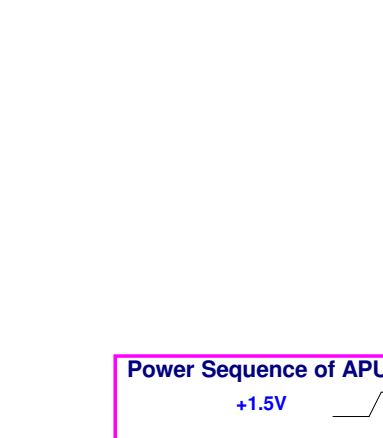
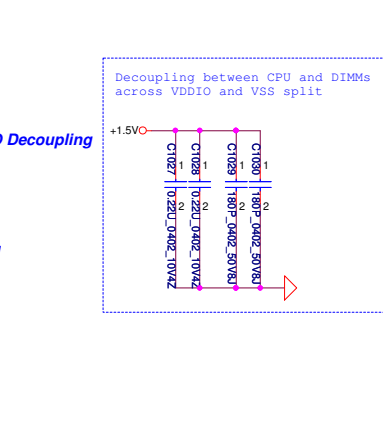
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Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2	
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16	

+CPU_CORE_NB Decoupling



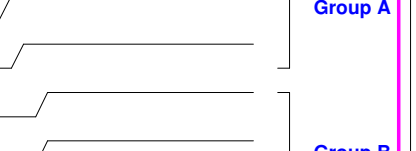
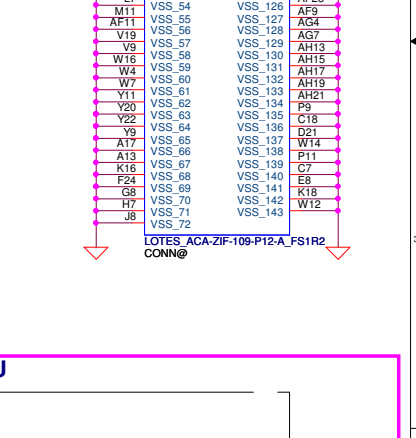
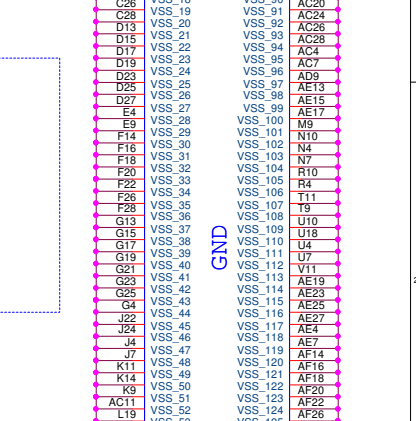
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Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2	
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16	

+CPU_CORE Decoupling

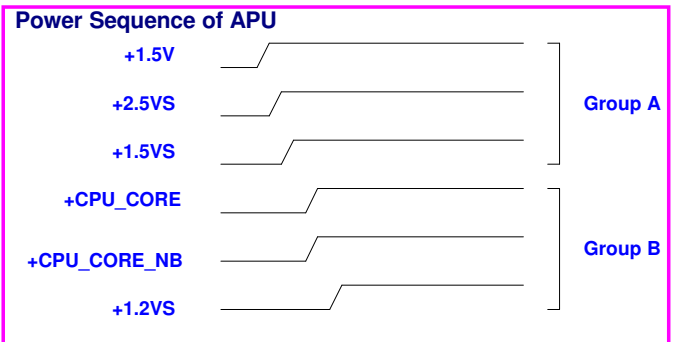


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Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2	
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16	

+CPU_CORE Decoupling



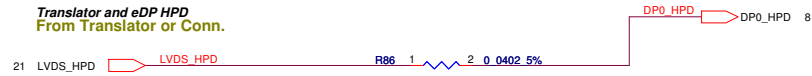
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Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2	
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16	



HPD

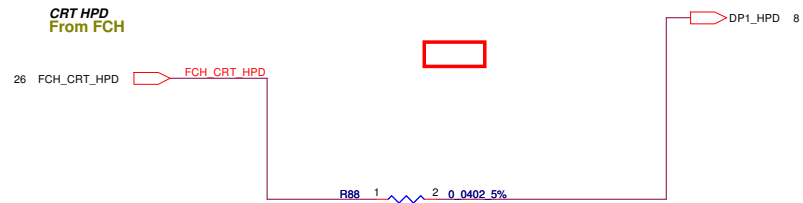
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Translator and eDP HPD
From Translator or Conn.



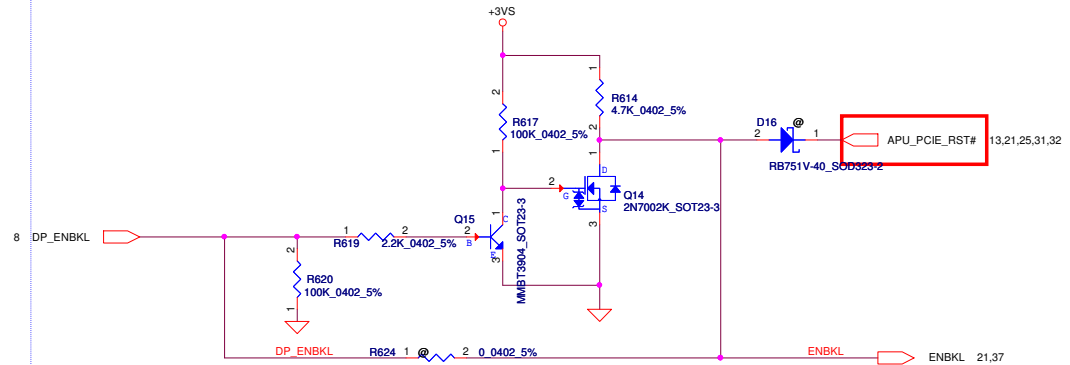
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CRT HPD
From FCH



Panel ENBKL

LA-8124 no use this DP_ENBKL.



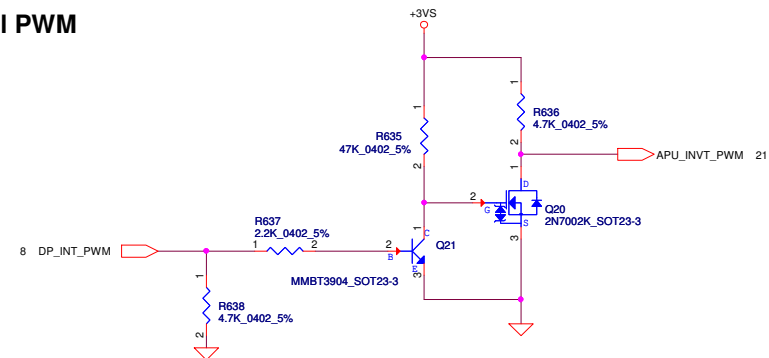
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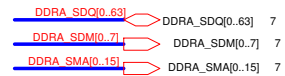
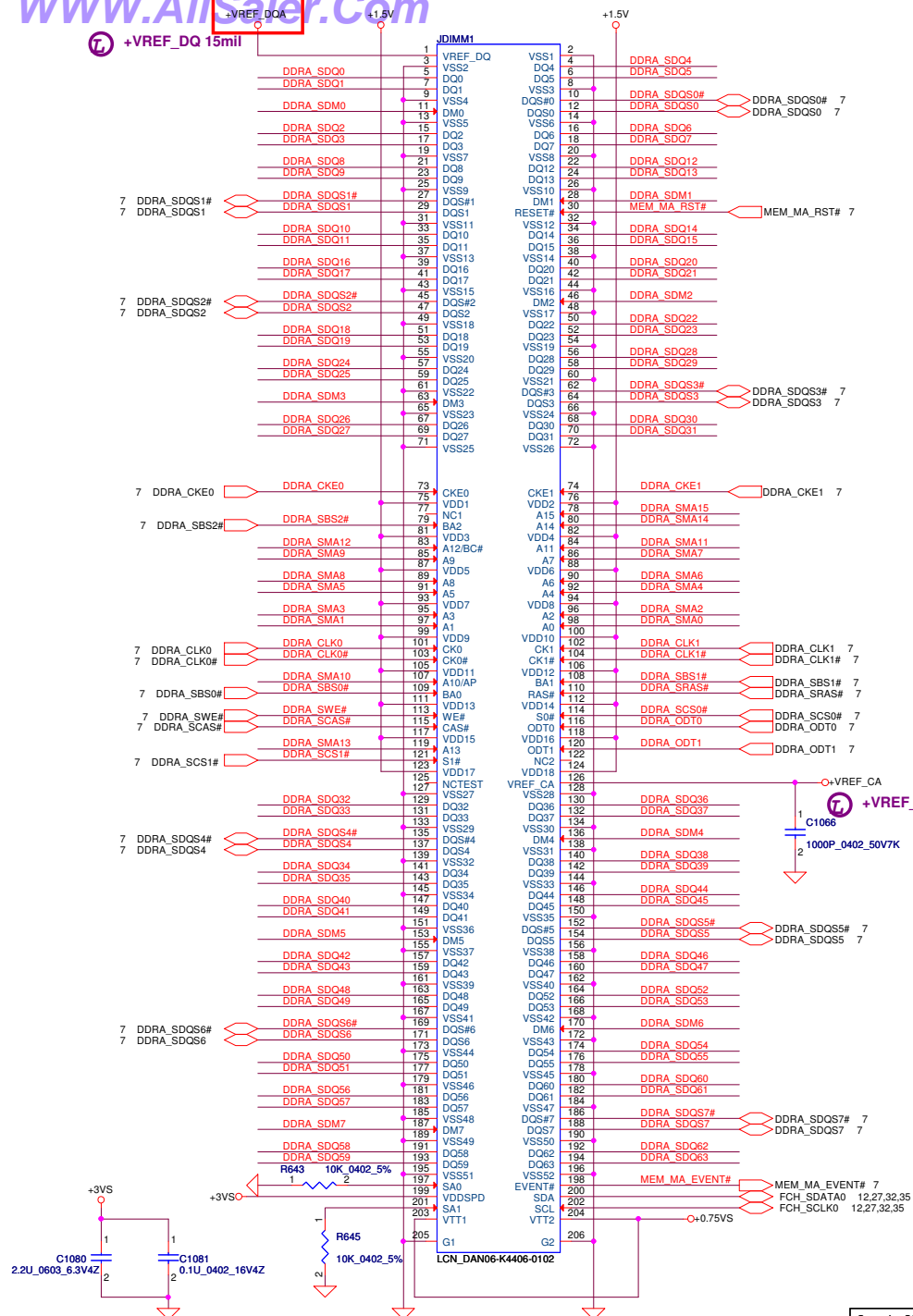
eDP Panel ENVDD

Del eDP panel control

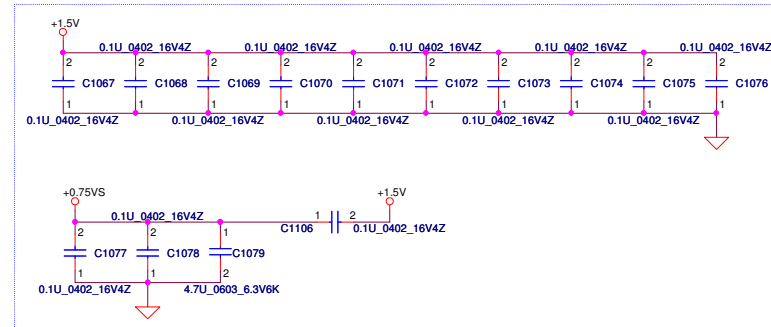
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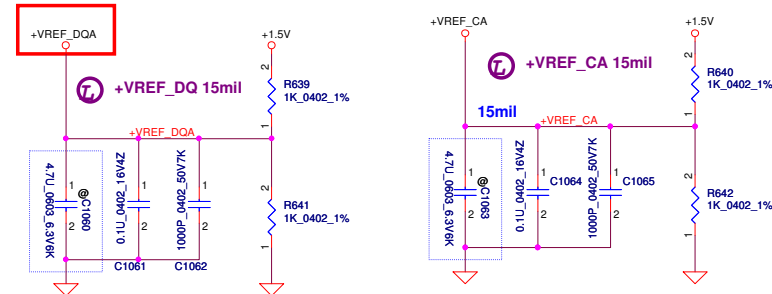
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Place near DIMM1

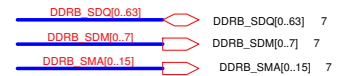
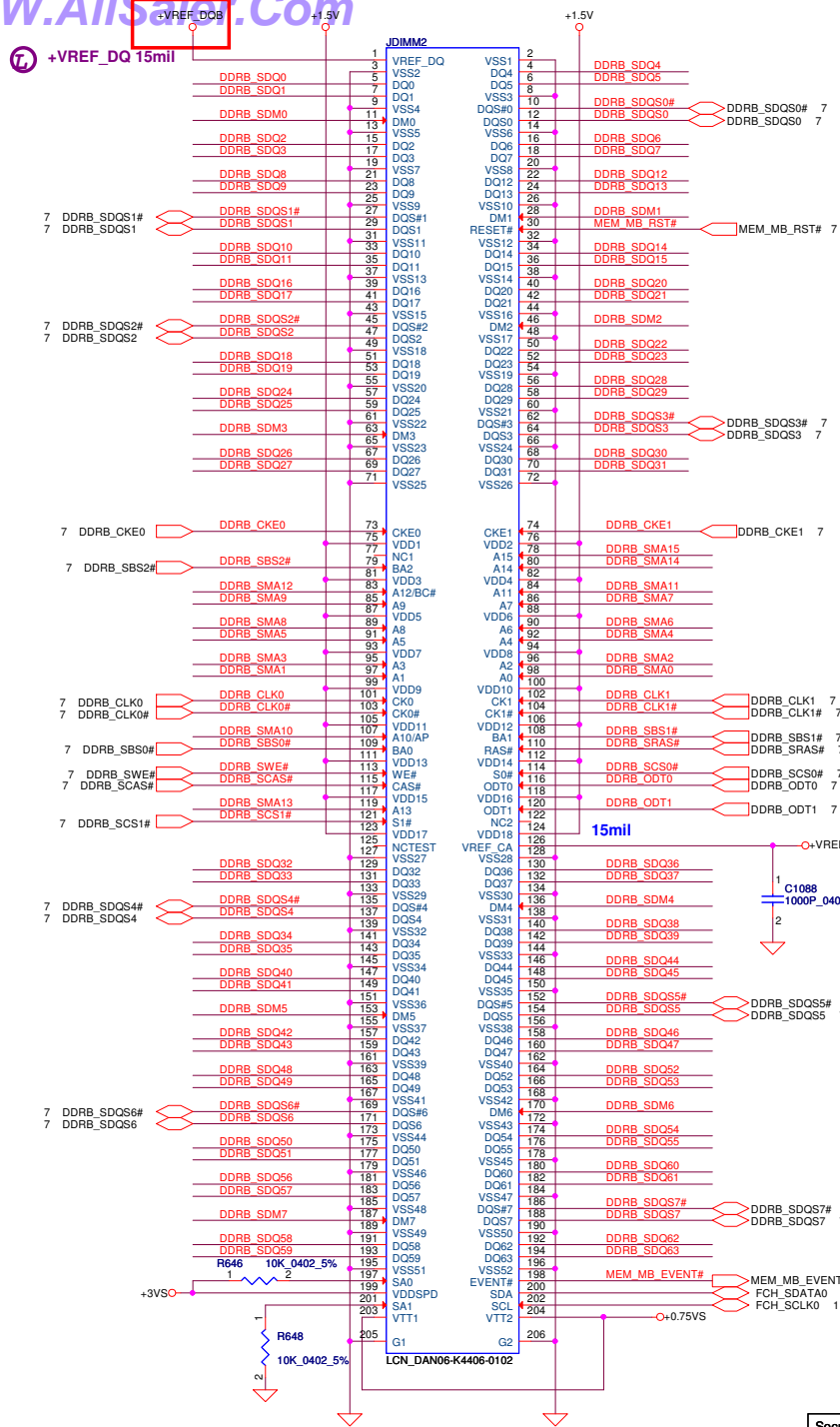


11/14 Change net name

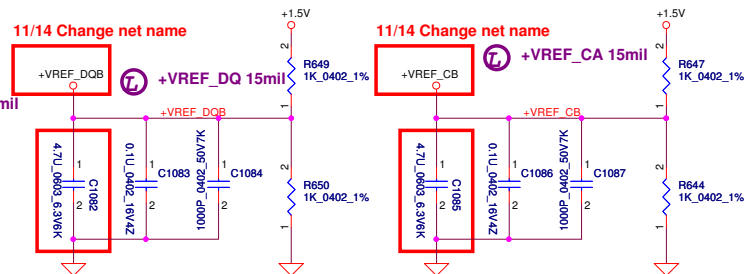
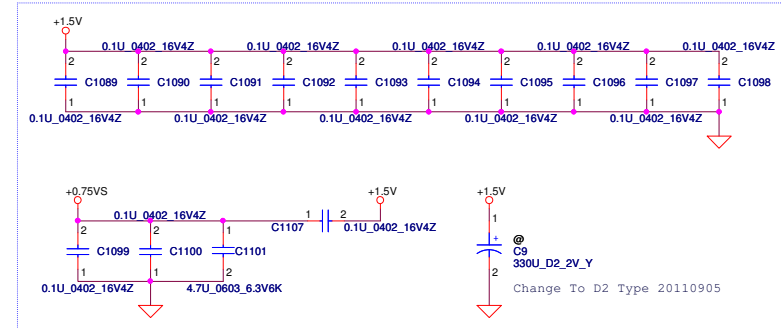


DIMM_A REV H:4mm
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Place near DIMM2

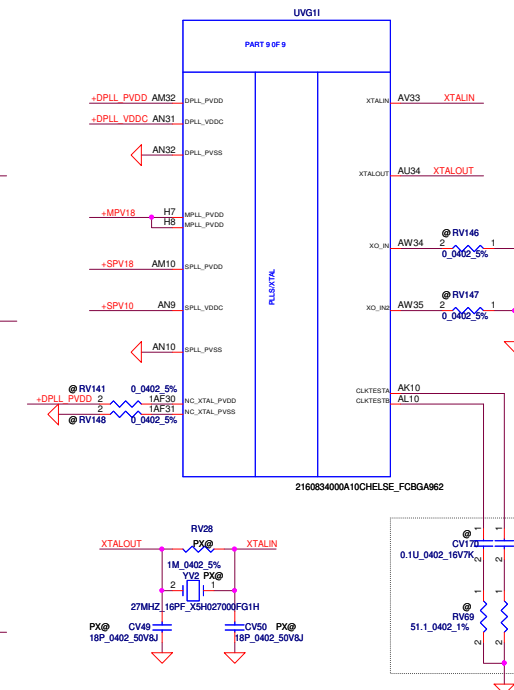
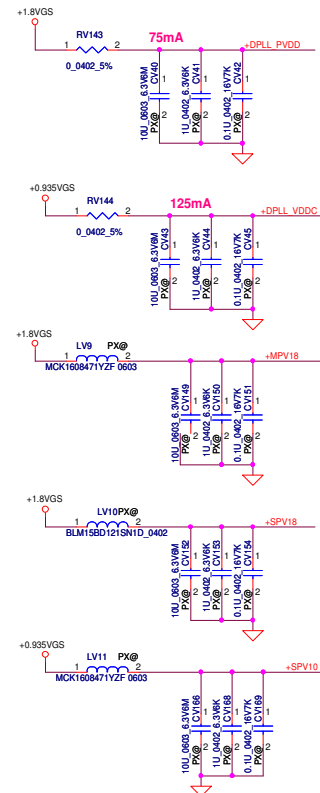
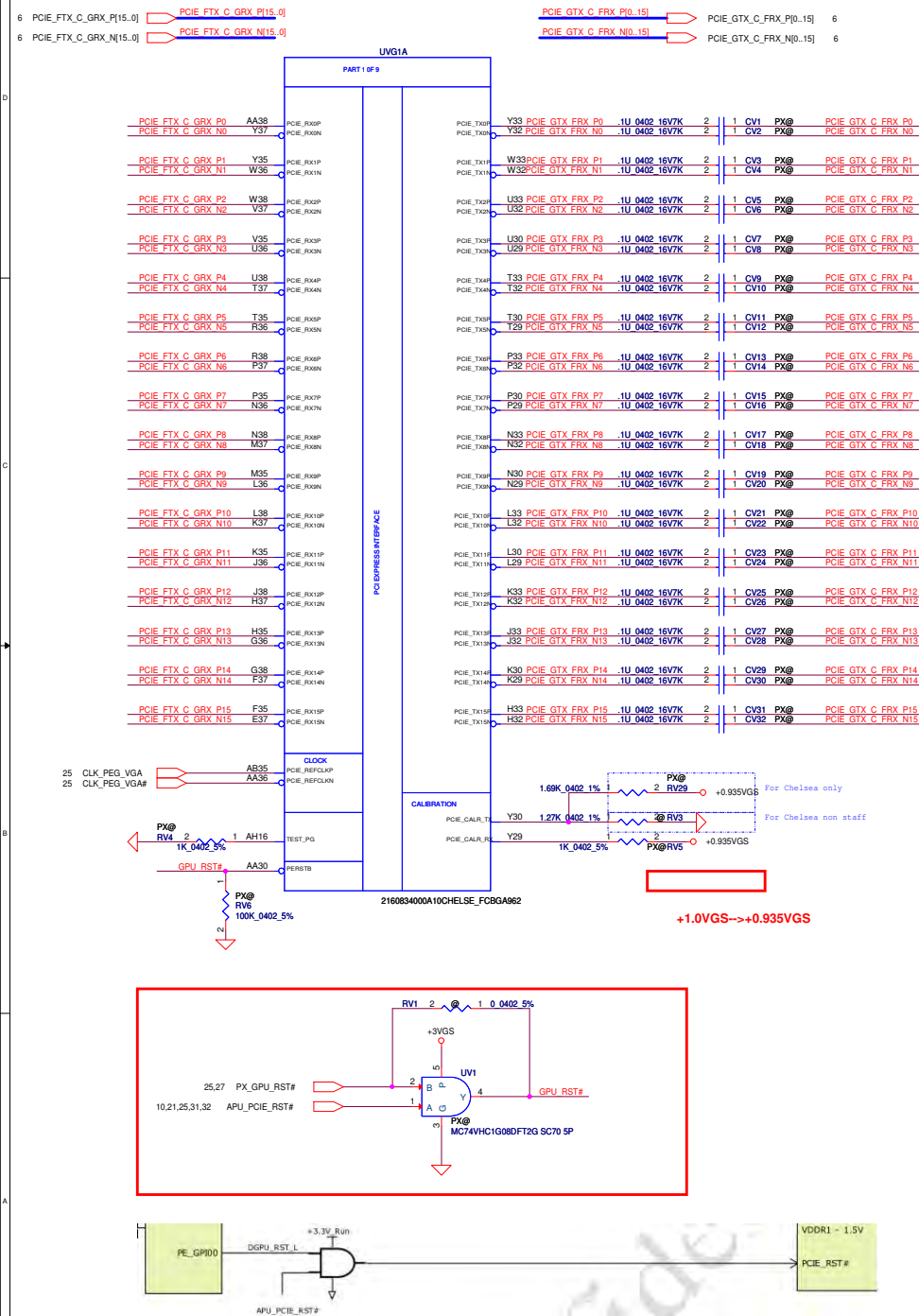


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LVDS Interface

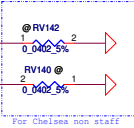


route 50ohms single-ended/100ohms diff
and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

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Size	C	Document Number	QCL51 LA-8712P	Rev 0.1
Date	Monday, November 28, 2011	Sheet	13	of 56



@RV142
 1 0_0402_5% 2
 RV140 @
 2 0_0402_5% 1
 For Chelsea non staff



Classification	Compal Secret Data		
Date	2011/06/30	Deciphered Date	2013/06/30

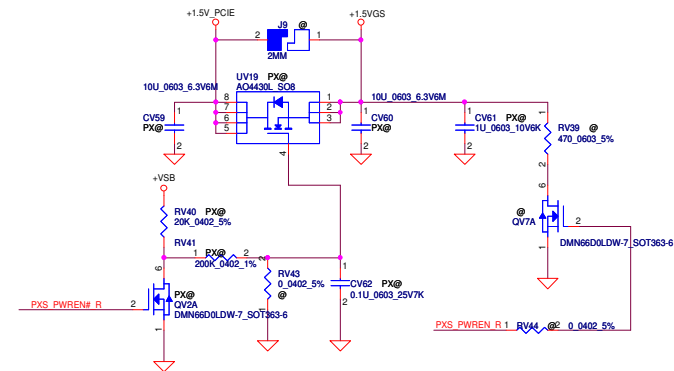
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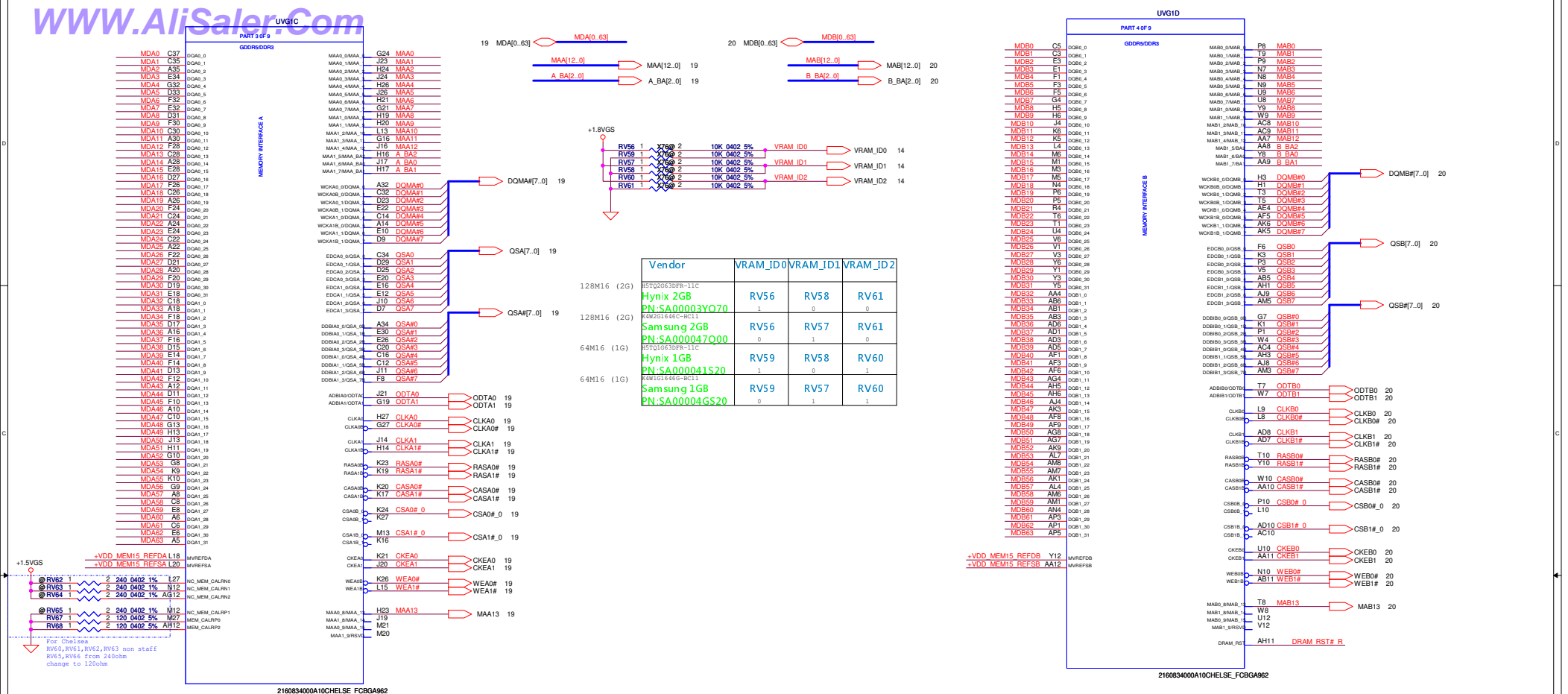
Compal Electronics, Inc.
ATI SeymourXT M2 Main MSIC
Part Number QCL51 LA-8712P
Date: November 09, 2011 | Sheet 14 of 22

GPU_Reset
PWREN



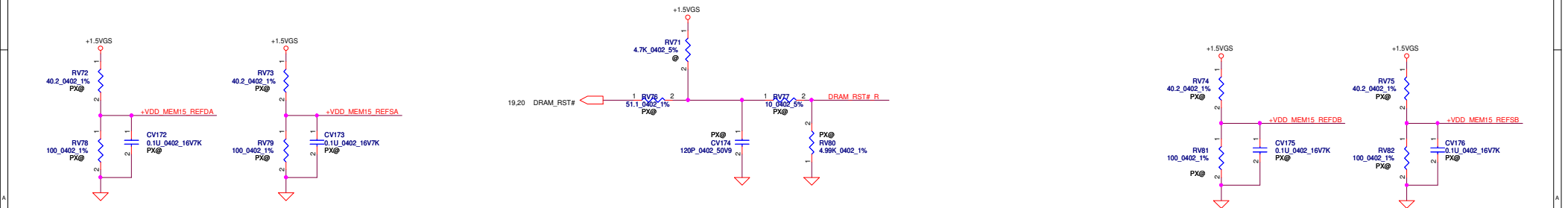
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[illegible]

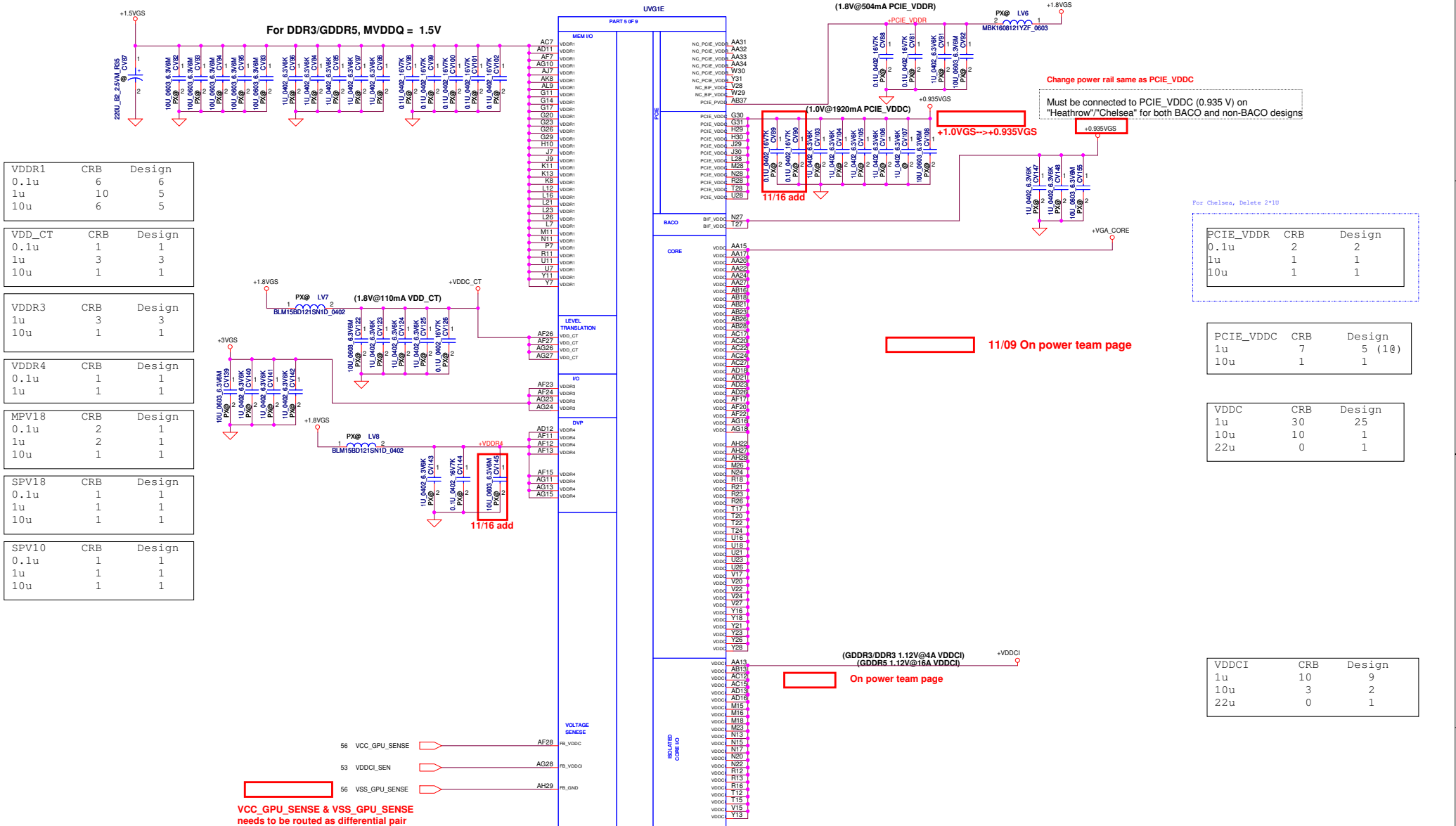


This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM load and board to pass Reset Signal Spec.

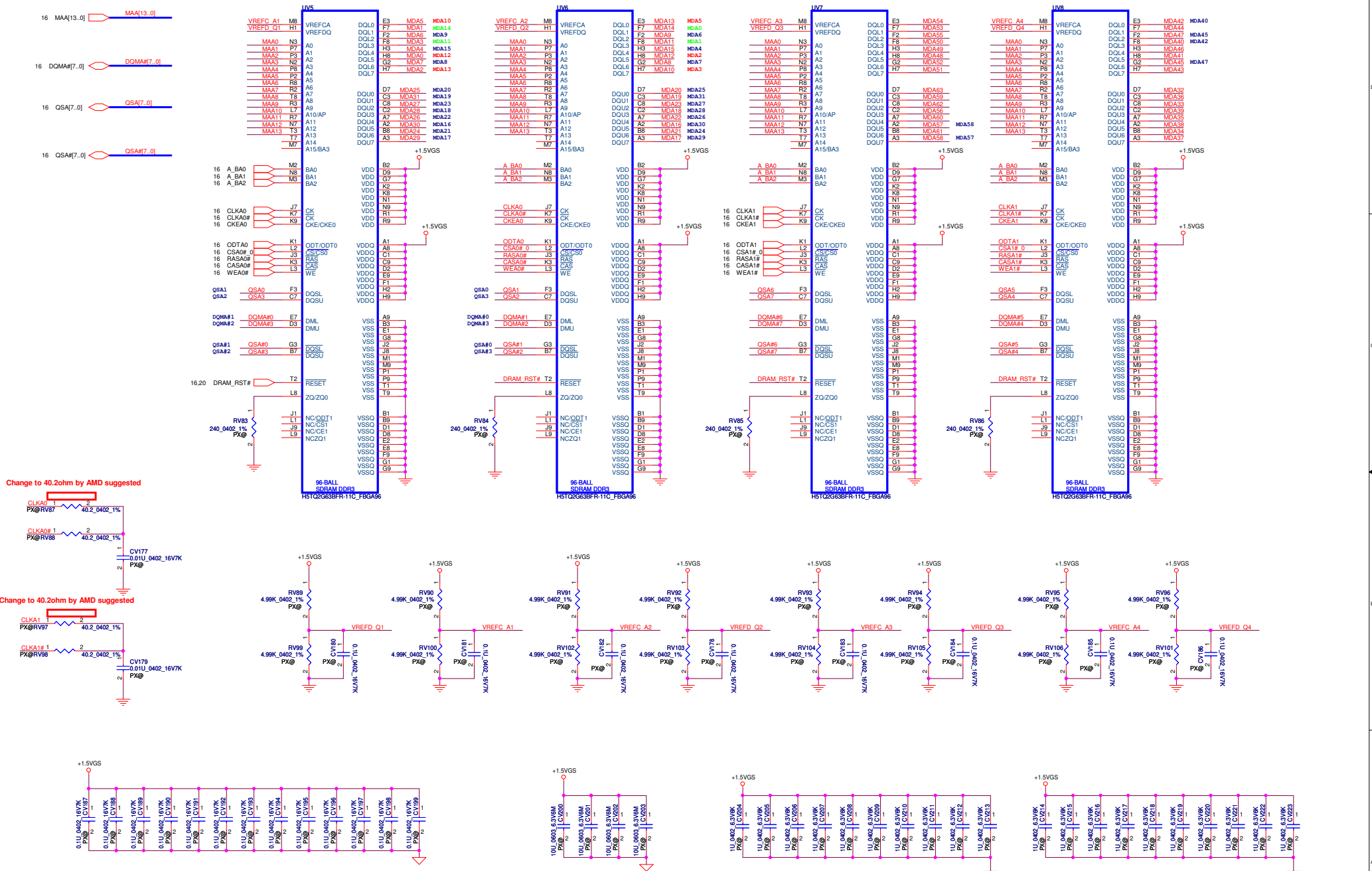
Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

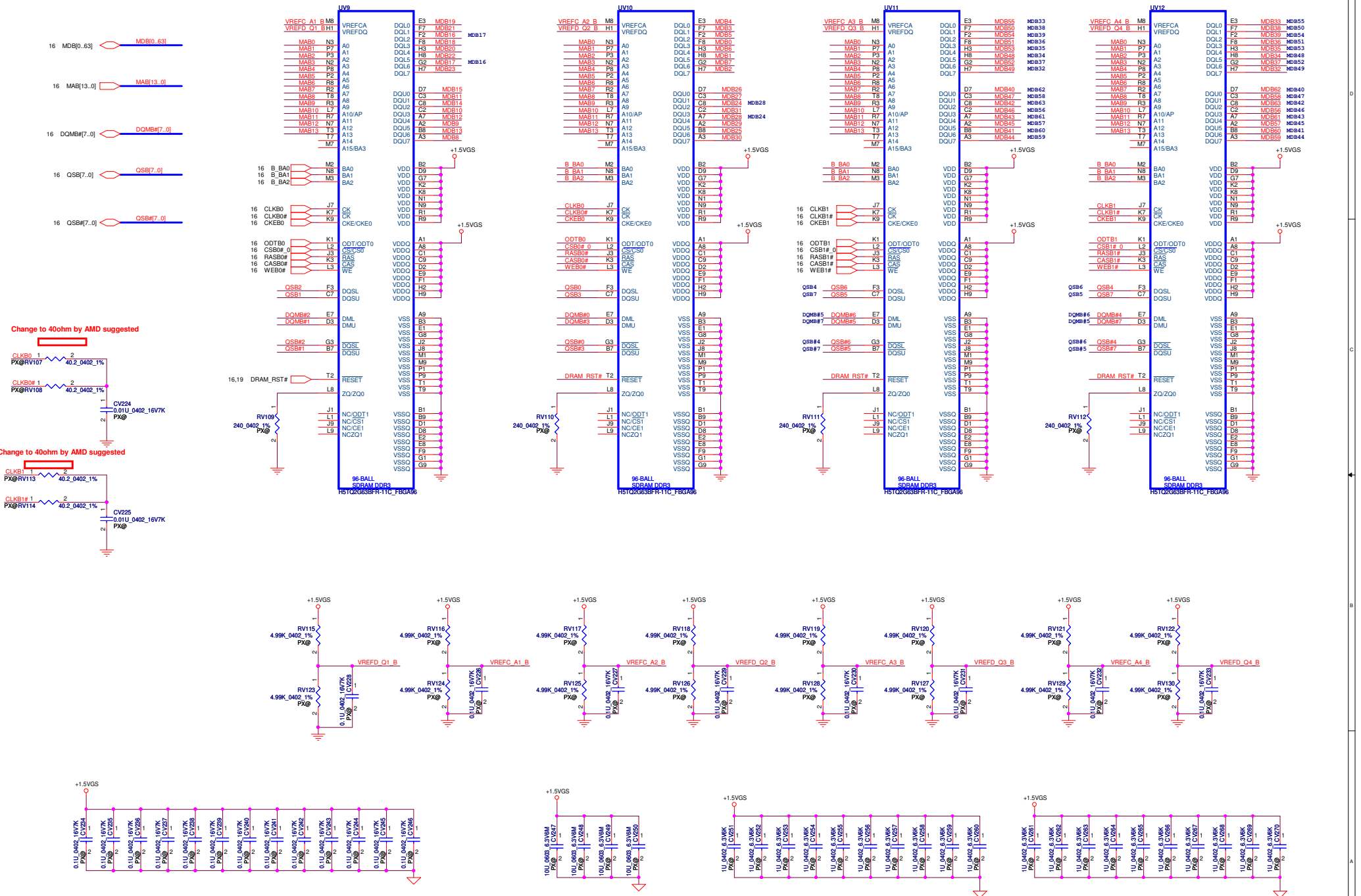


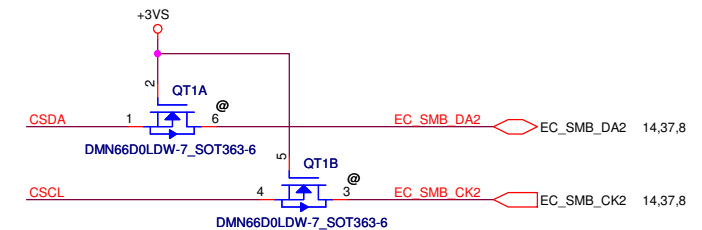
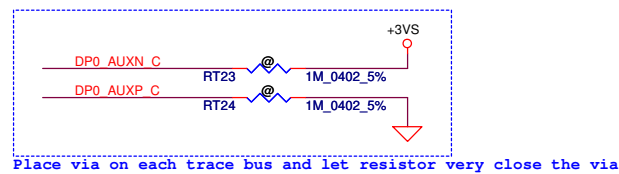
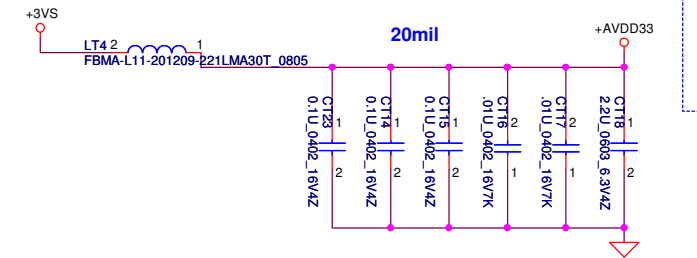
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Issued Date		2011/06/30	Deciphered Date		2013/06/30	
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				ATI SeymourXT M2 MEM IF		
				Size C	Document Number	Rev 0.1
				QCL51 LA-8712P		
Date:		Monday, November 28, 2011		Sheet	16	of 56



VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

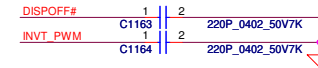
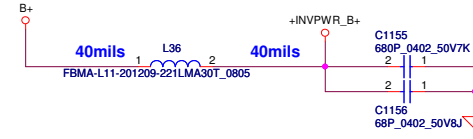
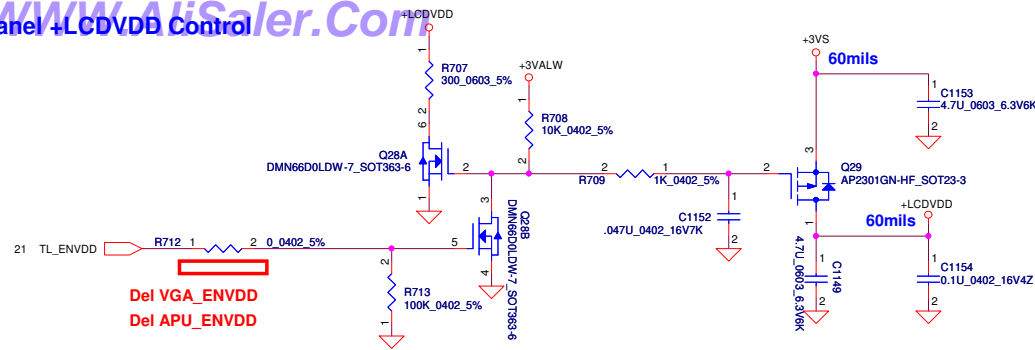






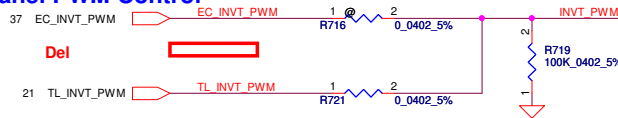
Security Classification	Compal Secret Data					
Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	LVDS Translator - ANX3112X	
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				OCL51 LA-8712P Date: Monday, November 28, 2011 Sheet 21 of 56		

Panel +LCDVDD Control

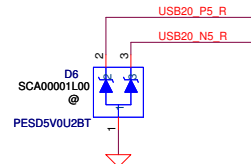
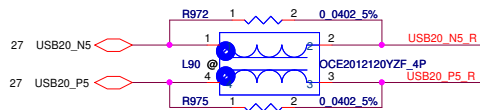


Panel Backlight Control

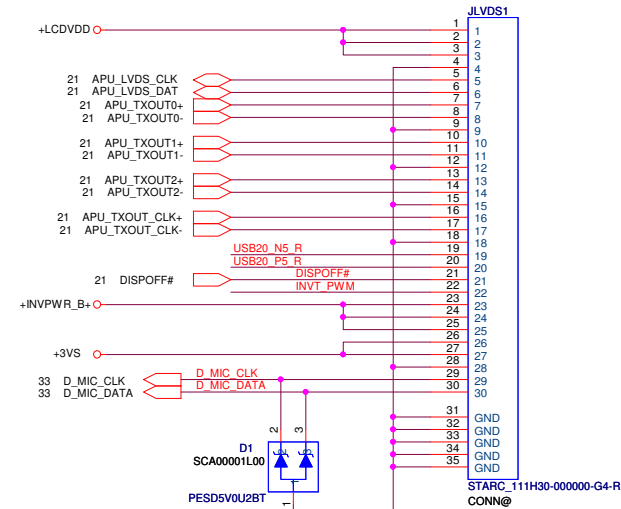
Modify and change to page 21



<Translator LVDS Output>



LVDS Connector

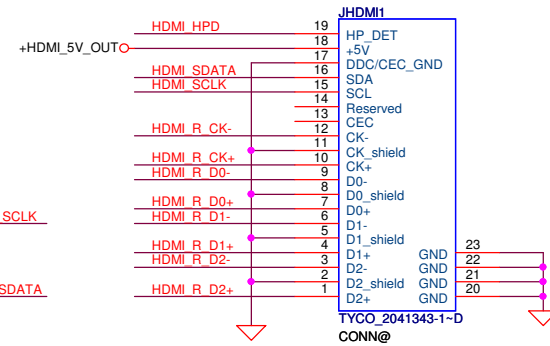
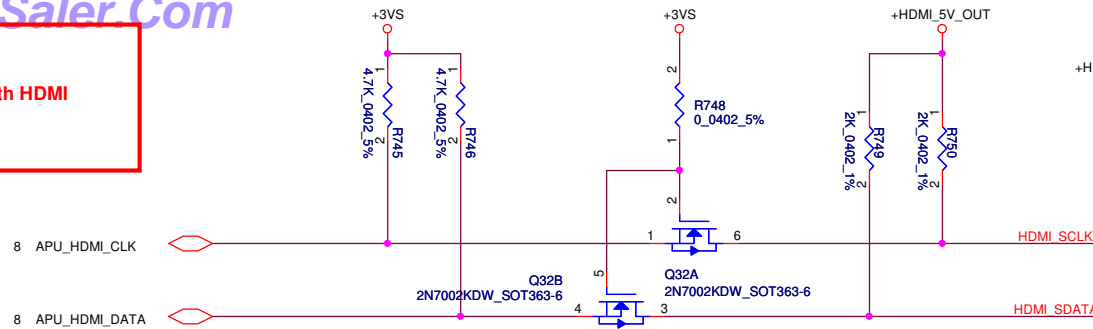


no updated.

11/10 follow QCL50

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	LVDS/eDP Connector
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				Customer	QCL51 LA-8712P
Date:				Monday, November 28, 2011	Sheet 22 of 56

Combine with HDMI

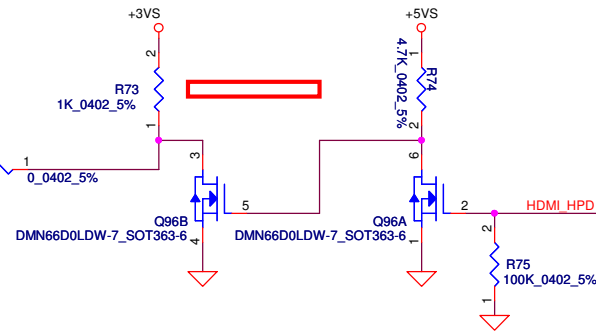


11/05 update footprint.

Del VGA_HDMI_DET

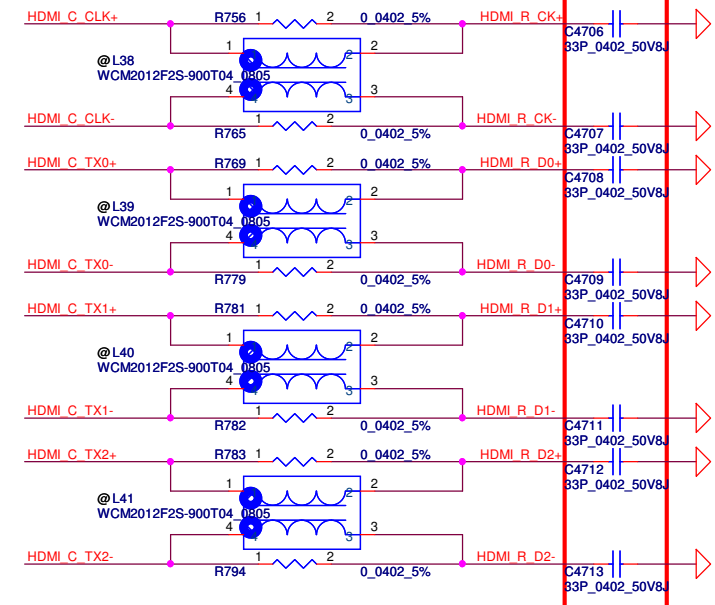
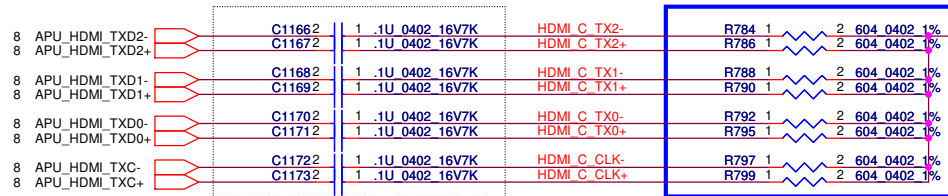
For APU_HDMI_HPD

8 DP2_HPD



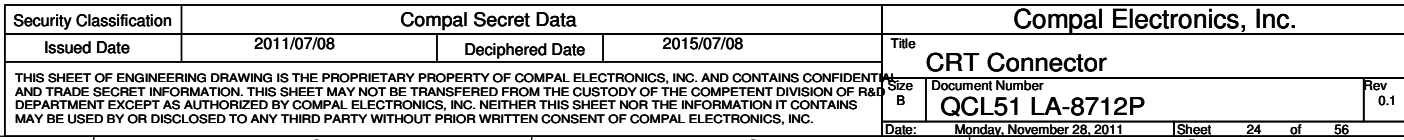
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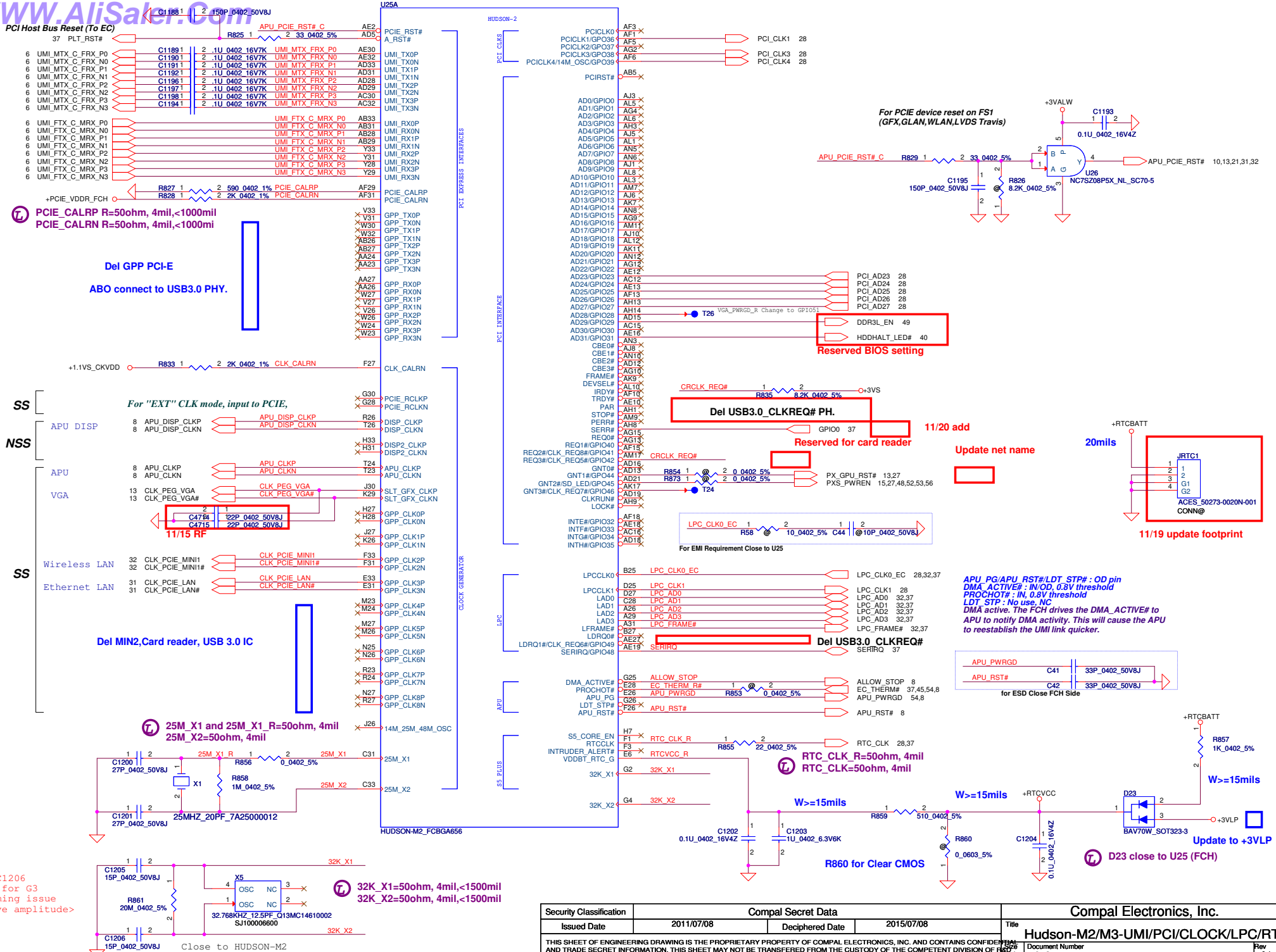
10/27 change to 604 ohm.



11/15 EMI
Near connector

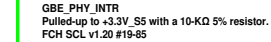
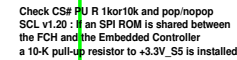
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						Size B		Document Number		Rev 0.1	
								QCL51 LA-8712P			
						Date:		Monday, November 28, 2011		Sheet 23 of 56	







Del WL_OFF#_2



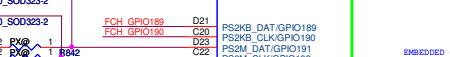
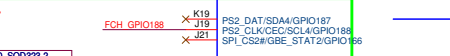
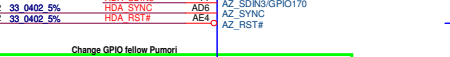
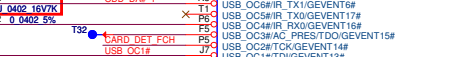
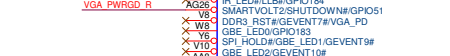
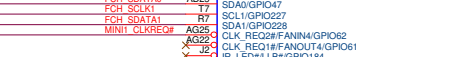
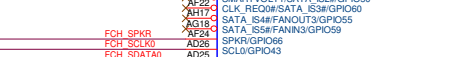
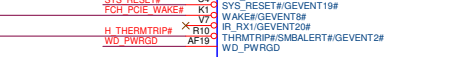
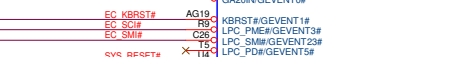
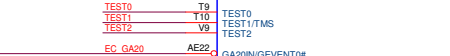
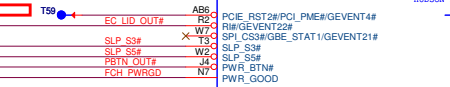
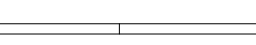
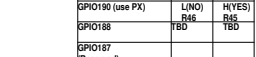
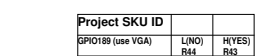
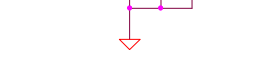
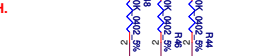
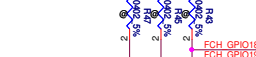
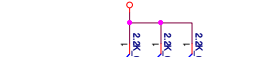
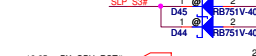
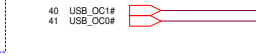
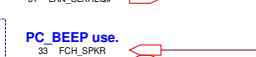
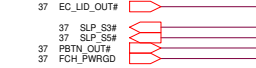
Removed RGMII/MII support and updated termination requirements for GBE_COL, GBE_CRS, GBE_RXERR and GBE_MDIO when RGMII/MII interface is not used.
FCH DgV1.20 / SCL v1.20



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				Customer	
				Document Number	Rev
				QCL51 LA-8712P	0.1
Date:		Monday, November 28, 2011		Sheet	26 of 56

FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

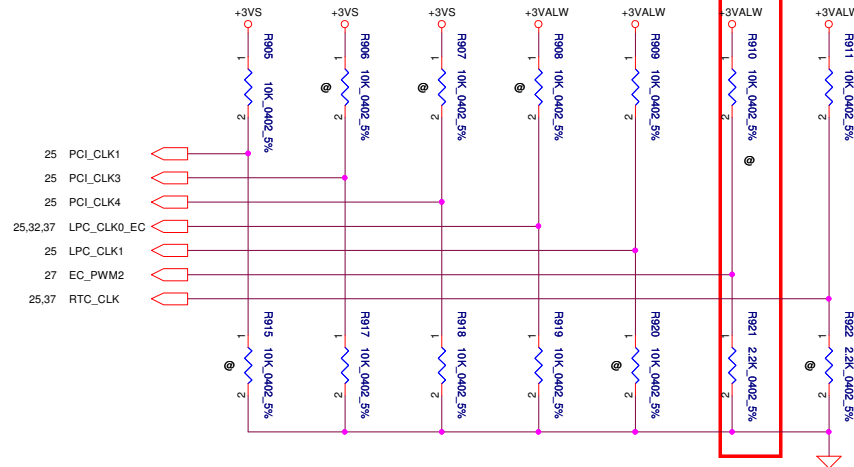
Del FCH_PCIE_RST#



Change to SPI

STRAP PINS

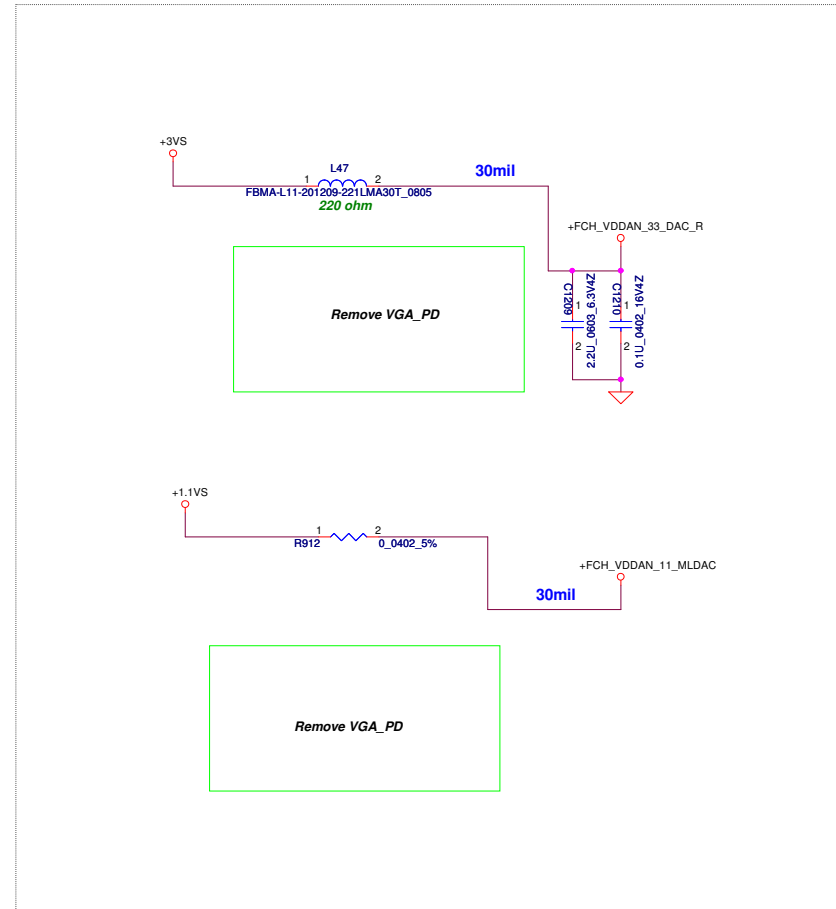
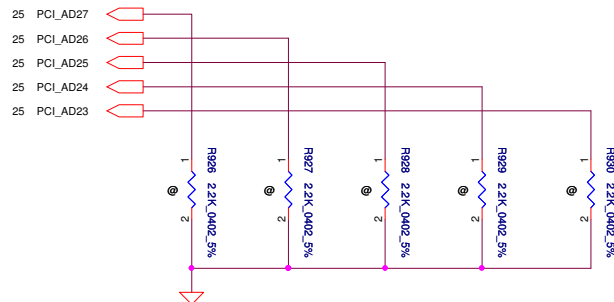
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

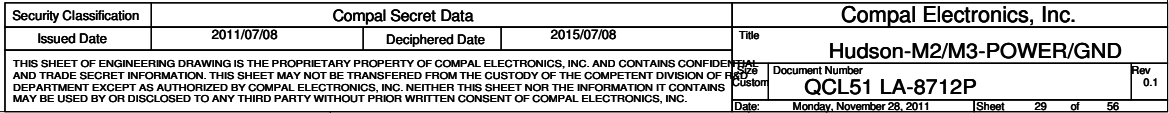


DEBUG STRAPS

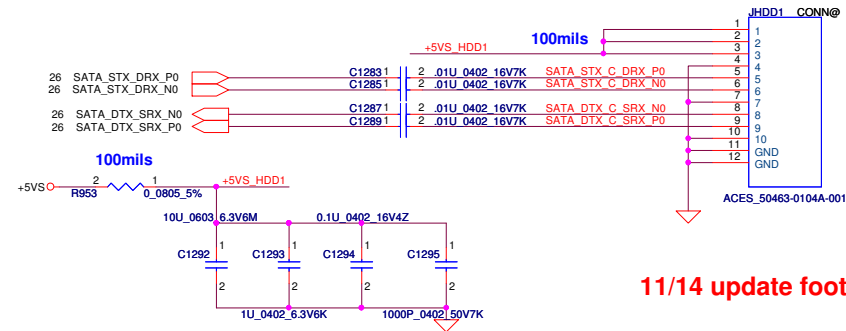
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

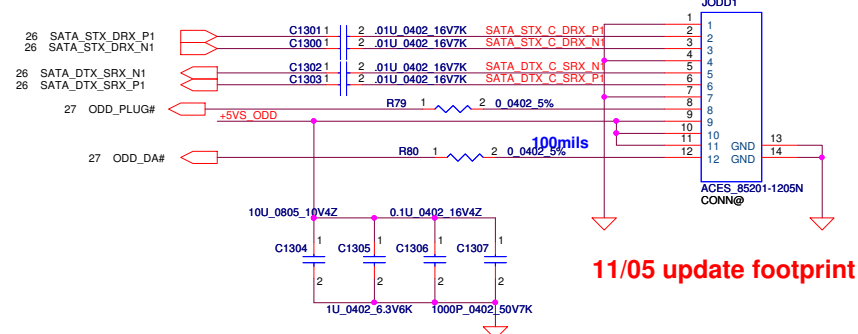
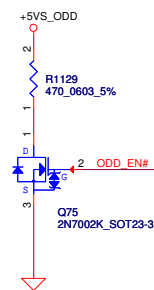
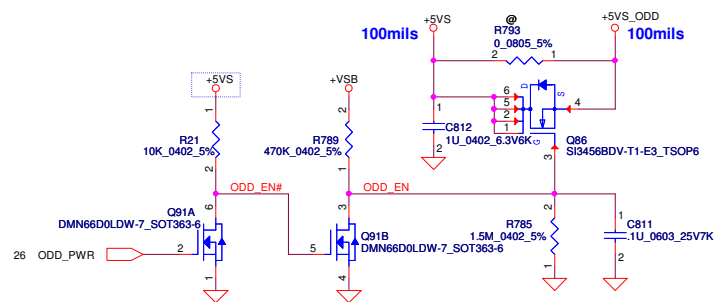




SATA HDD1 Conn.

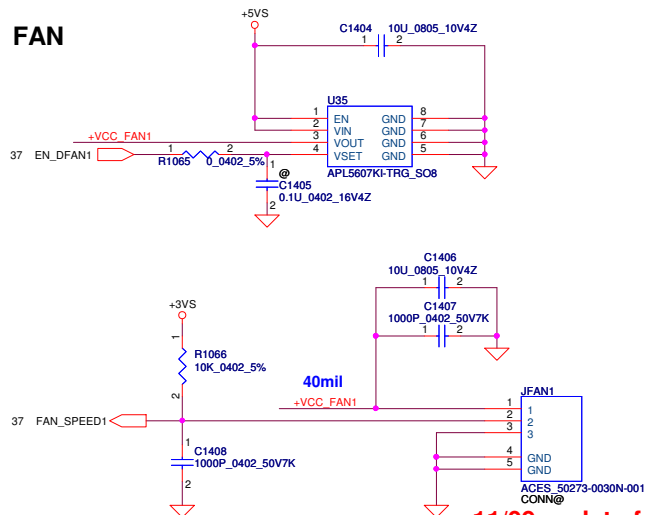


11/14 update footprint



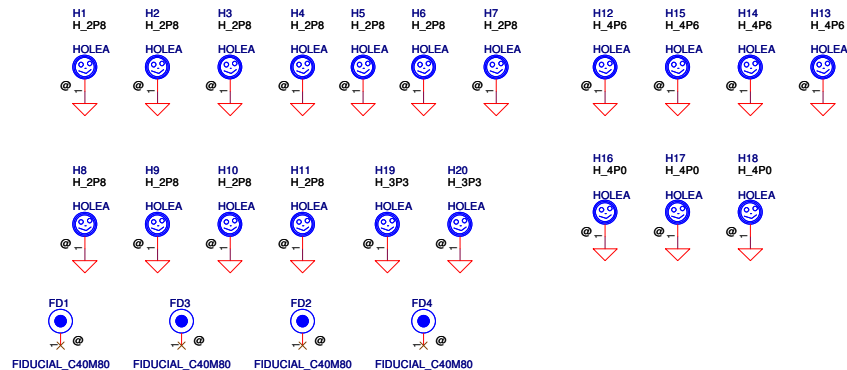
11/05 update footprint

FAN



11/09 update footprint to VT.

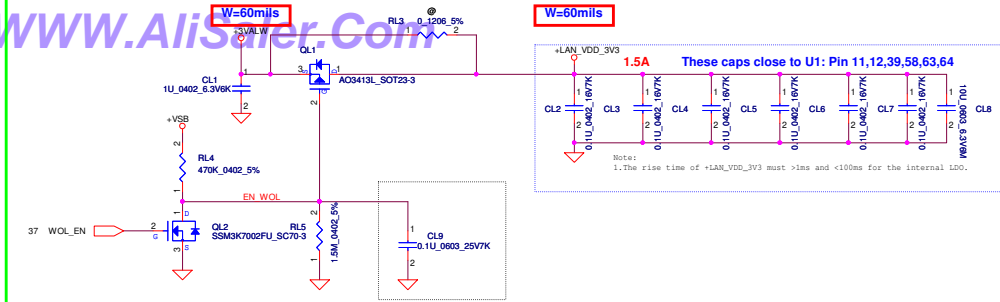
Screw Hole



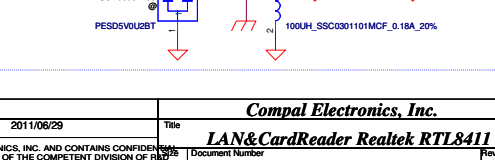
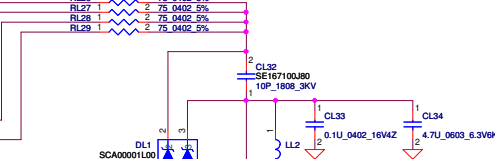
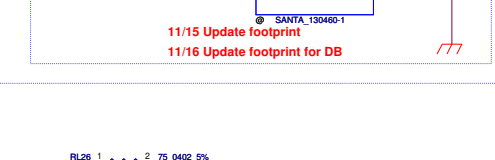
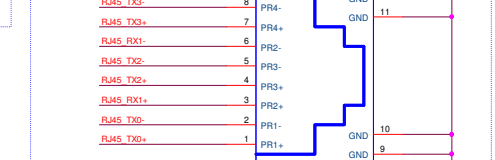
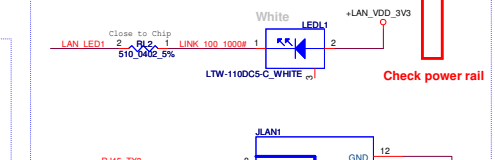
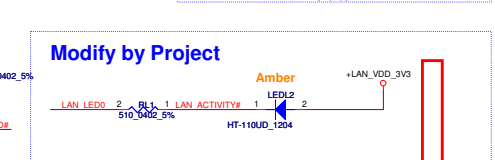
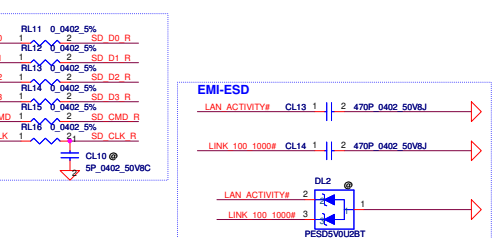
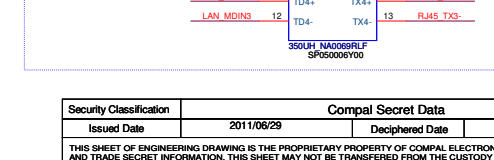
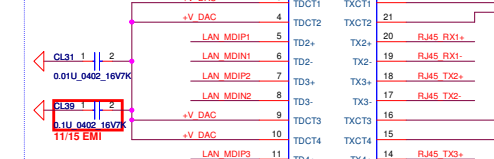
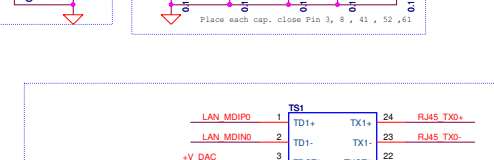
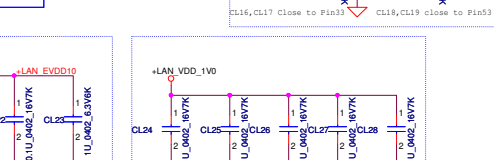
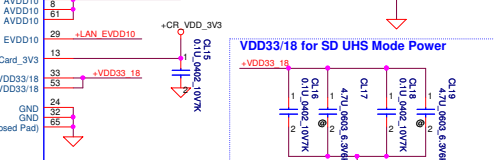
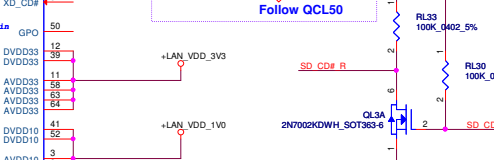
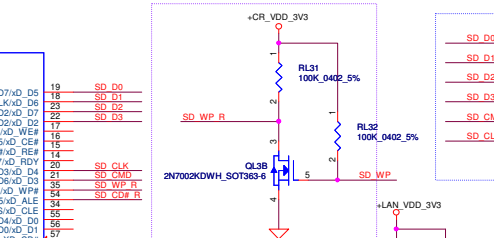
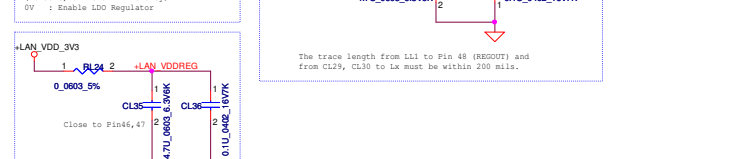
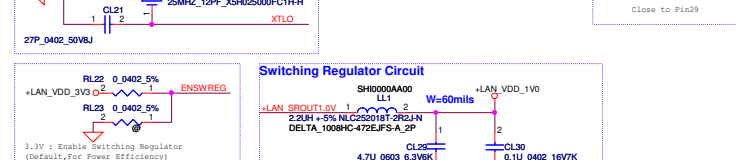
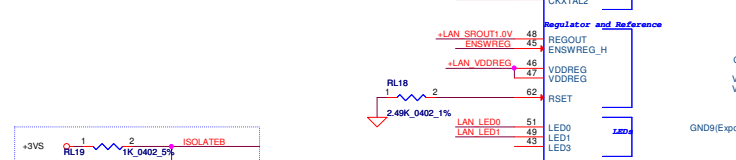
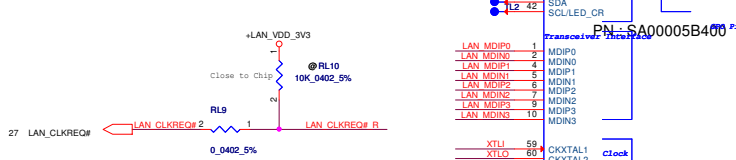
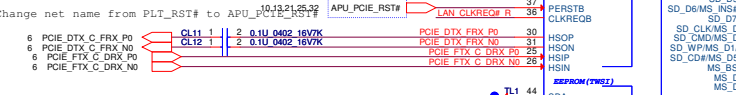
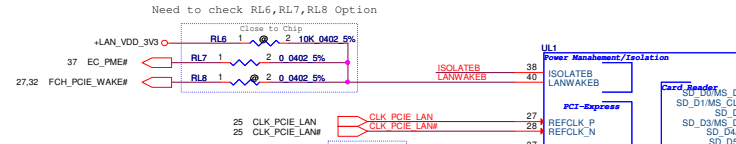
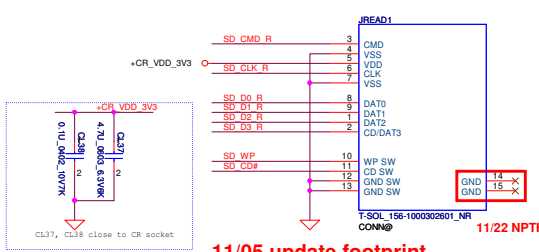
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				QCL51 LA-8712P		0.1
				Date	Monday, November 28, 2011	Sheet

W=60mils

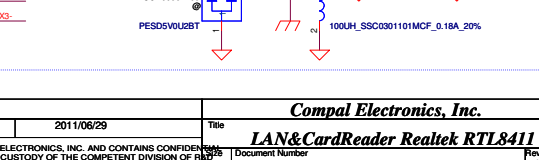
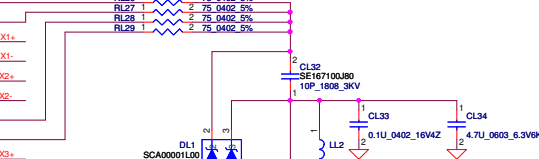
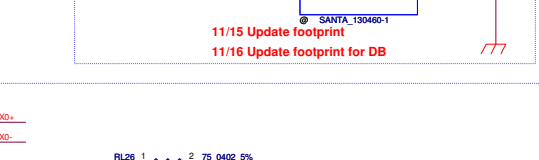
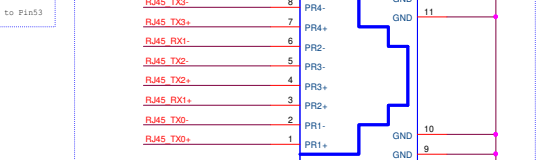
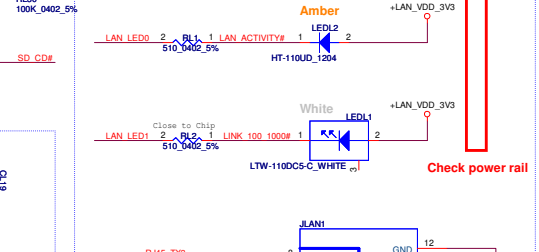
W=60mils



Modify by Project



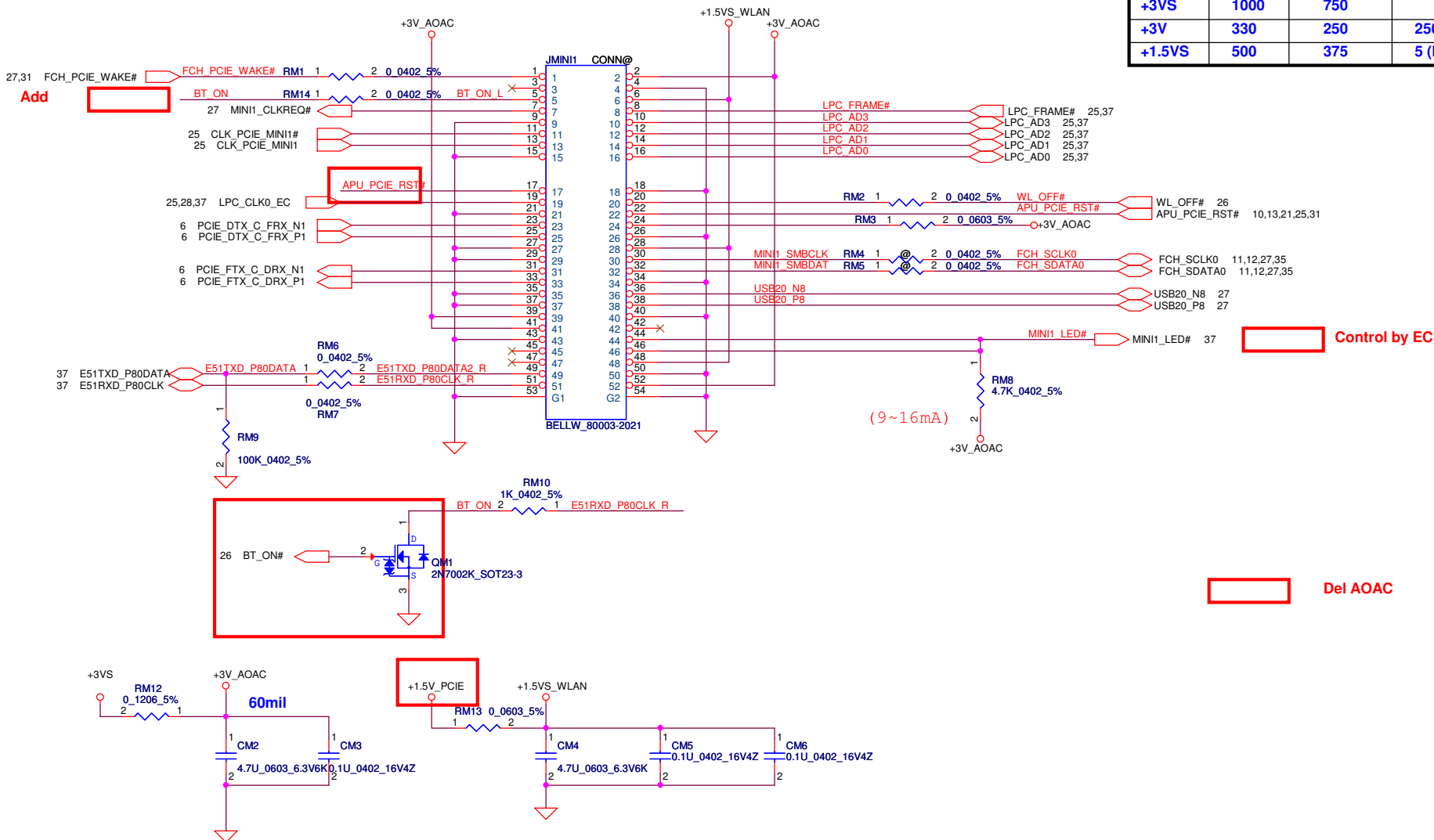
Modify by Project



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WLAN

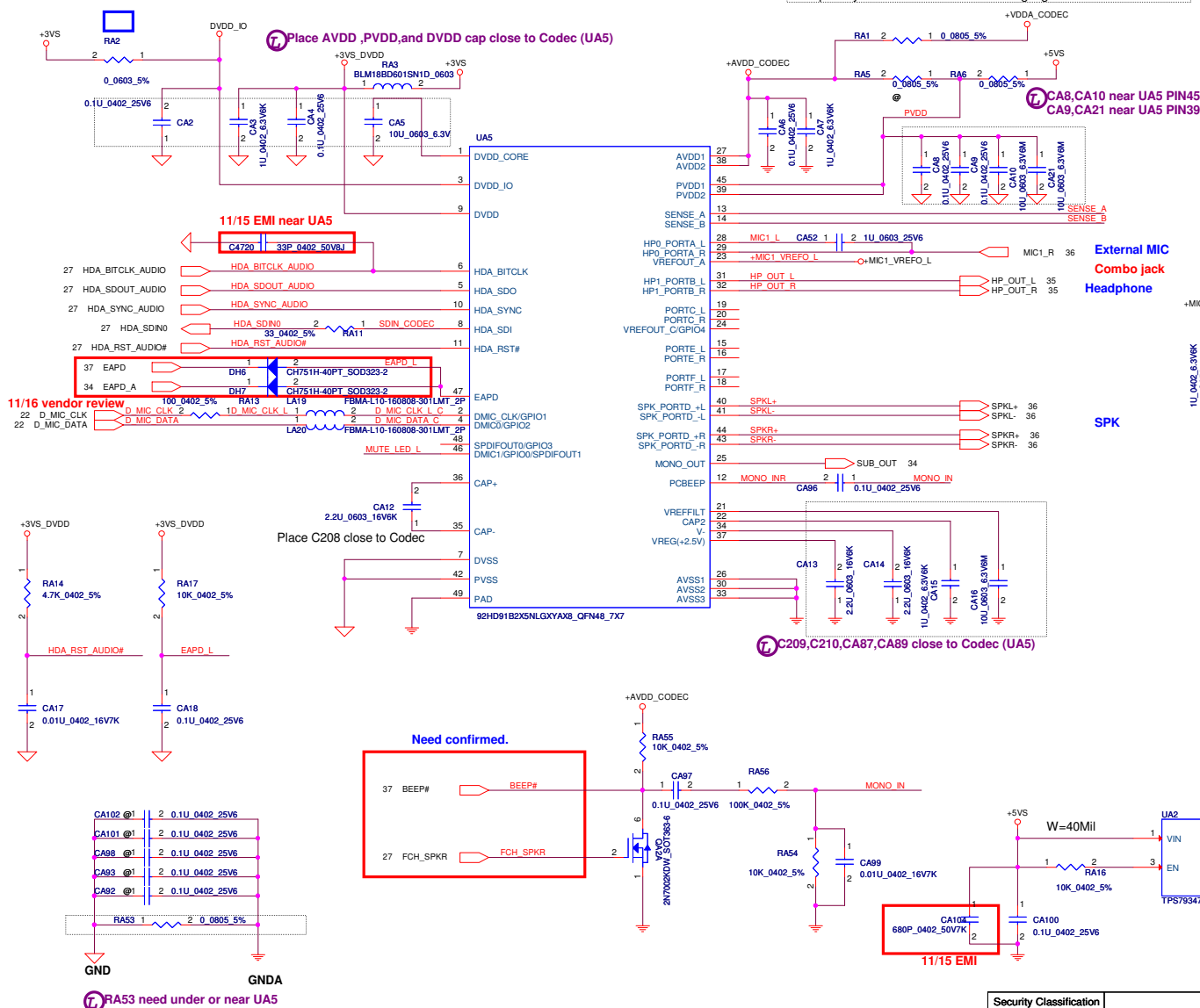
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



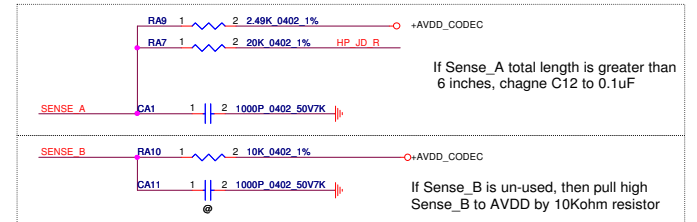
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	MINI1 CARD (WLAN) / MINI2 CARD (Option)	
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RA2 0805-->0603

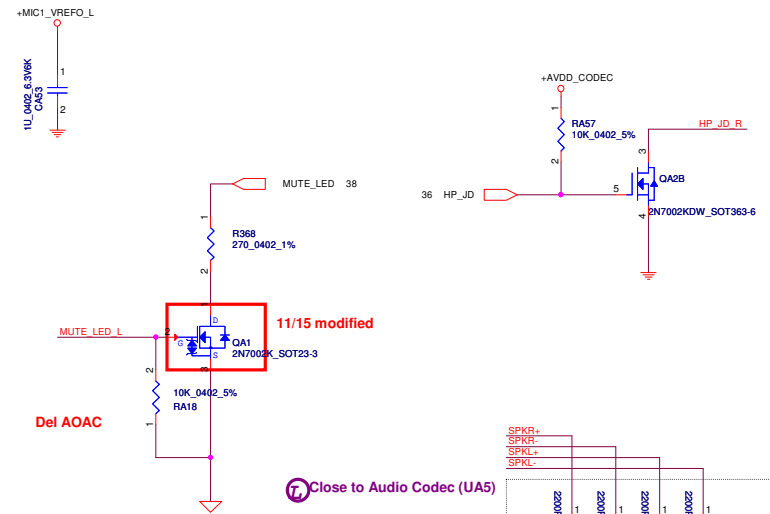
Place AVDD, PVDD, and DVDD cap close to Codec (UA5)



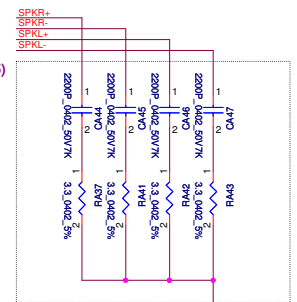
PLACE CLOSE TO UA5 PIN 13



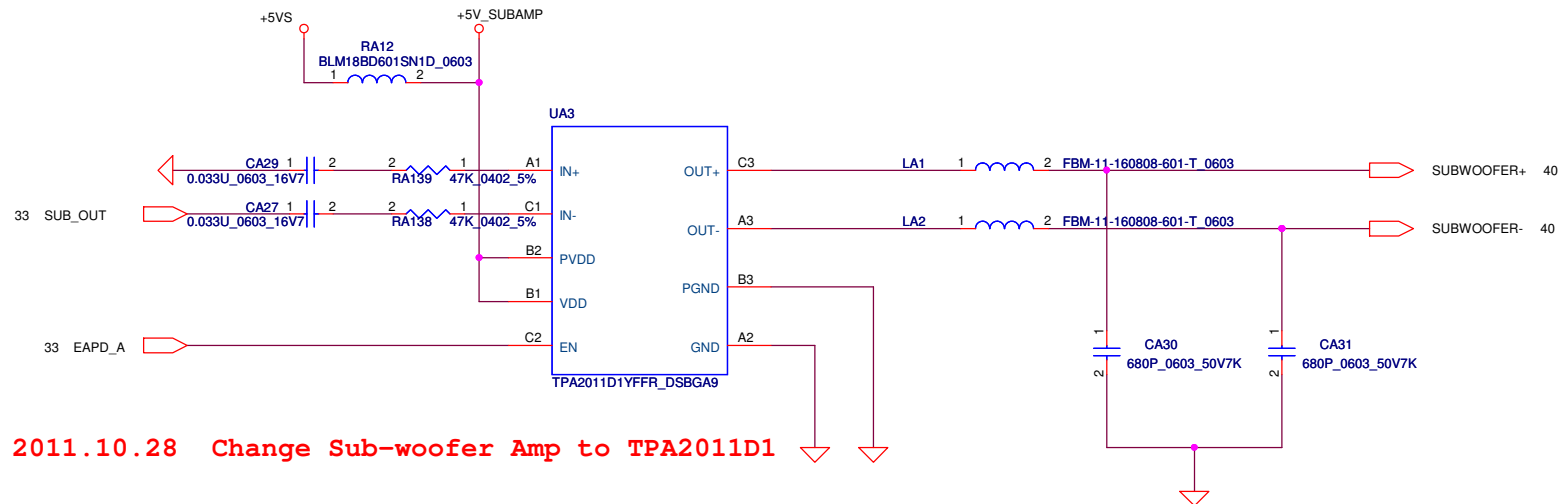
PLACE CLOSE TO UA5 PIN 14



Close to Audio Codec (UA5)

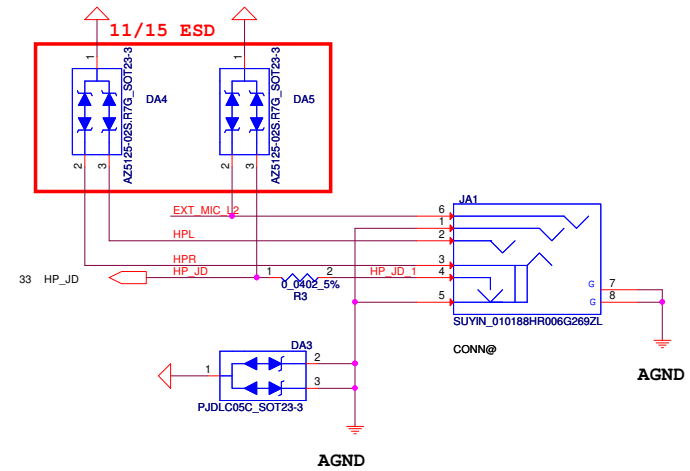
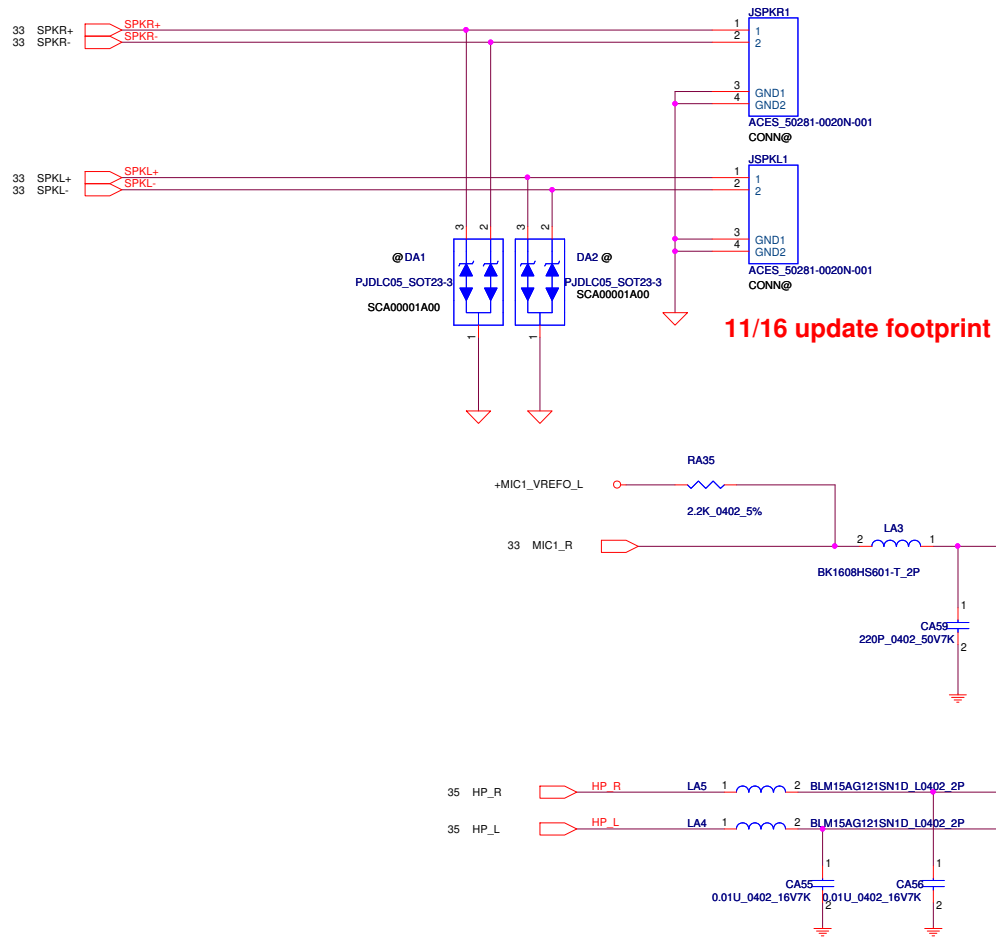


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Audio IDT 92HD91
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SPK conn



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Issued Date	2009/04/07	Deciphered Date	2012/10/21	Title	Audio SPK Conn/Jack/MIC		
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WWW.AliSaler.Com

11/15 EMI

11/15 add for HW shut down

Del INT_VGAPWR_ON

Del GPIO18

Del PWR_SUSP_LED#

020 modify Remove X2 20110915

11/09

KB932QF-A0_LQFP128_14X14
Part Number = SA000055100

20mil

BLM18AG601SN1D_2P

Security Classification

Compal Secret Data

Issued Date 2011/07/08

Deciphered Date 2015/07/08

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Compal Electronics, Inc.

EC ENE KB930/9012

Size B

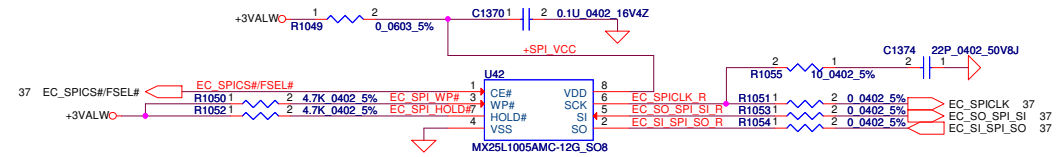
Document Number QCL51 LA-8712P

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Date Monday, November 28, 2011

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KB conn

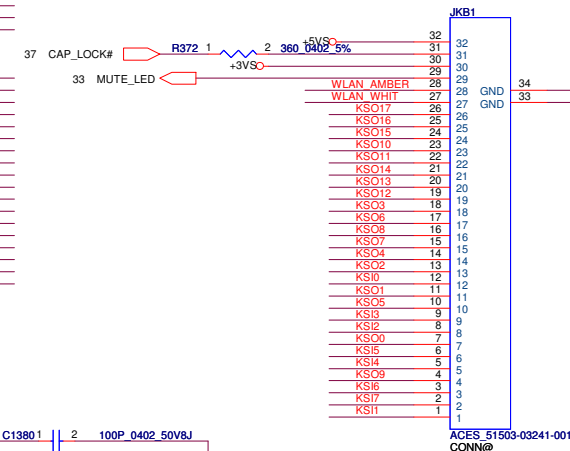
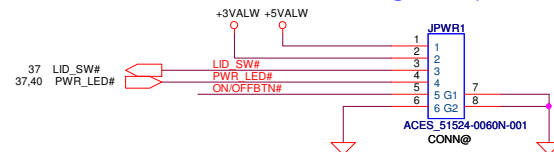


37 KSI[0..7]

37 KSO[0..17]

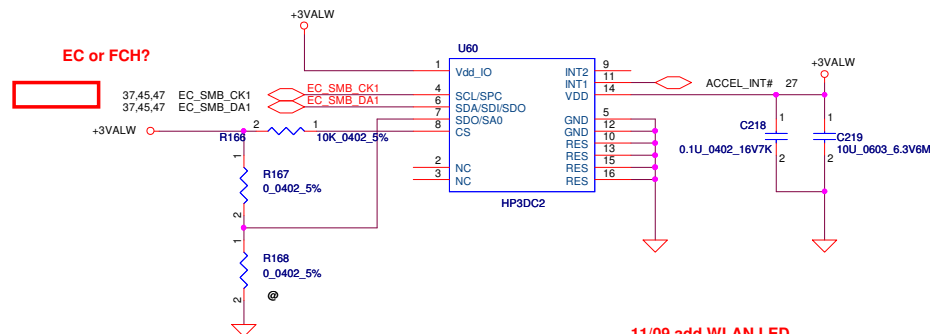
KSI7
KSI6
KSI5
KSI4
KSI3
KSI2
KSI1
KSI0

KSO17
KSO16
KSO15
KSO14
KSO13
KSO12
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KSO6
KSO5
KSO4
KSO3
KSO2
KSO1
KSO0

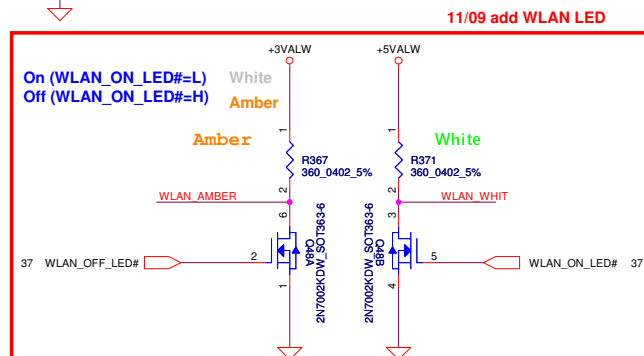


11/05 update footprint

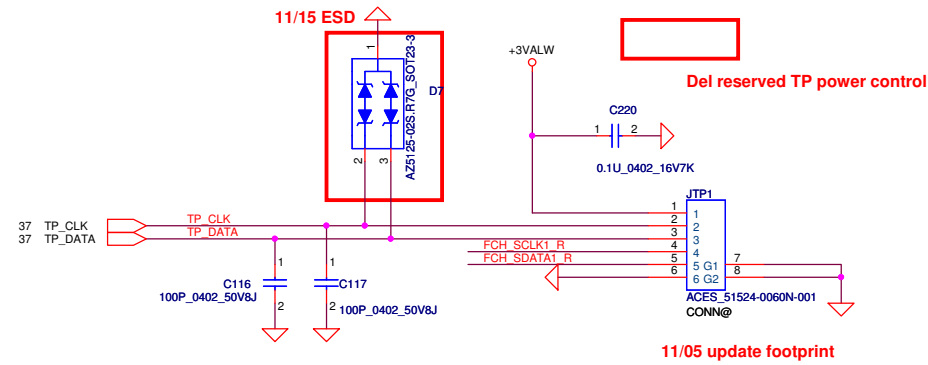
KSO15	C13801	2	100P_0402_50V8J
KSO14	C13831	2	100P_0402_50V8J
KSO13	C13841	2	100P_0402_50V8J
KSO12	C13861	2	100P_0402_50V8J
KSO10	C13881	2	100P_0402_50V8J
KSO11	C13901	2	100P_0402_50V8J
KSO10	C13921	2	100P_0402_50V8J
KS11	C13941	2	100P_0402_50V8J
KS12	C13961	2	100P_0402_50V8J
KS09	C13981	2	100P_0402_50V8J
KS13	C14001	2	100P_0402_50V8J
KSO8	C14021	2	100P_0402_50V8J
KSO3	C13891	2	100P_0402_50V8J
KS14	C13911	2	100P_0402_50V8J
KSO2	C13931	2	100P_0402_50V8J
KSO1	C13951	2	100P_0402_50V8J



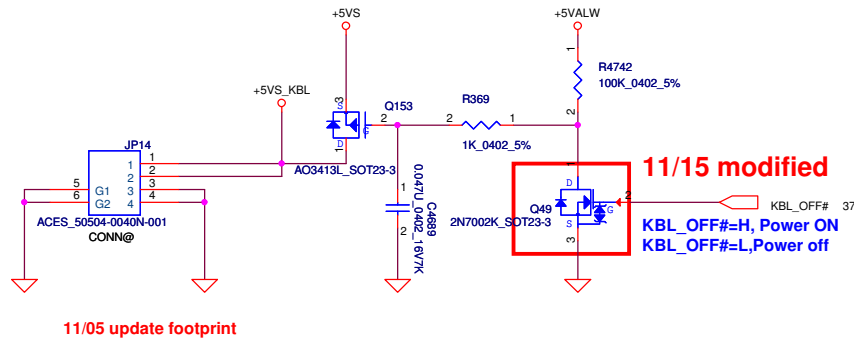
Part Number	Part Name	QTY	UOM	DESCRIPTION
KSO16	C13781	2	100P	0402 50V8J
KSO17	C13791	2	100P	0402 50V8J
KSO7	C13811	2	100P	0402 50V8J
KSO6	C13821	2	100P	0402 50V8J
KSO5	C13851	2	100P	0402 50V8J
KSO4	C13871	2	100P	0402 50V8J
KSO0	C13971	2	100P	0402 50V8J
KSI5	C13991	2	100P	0402 50V8J
KSI6	C14011	2	100P	0402 50V8J
KSI7	C14031	2	100P	0402 50V8J



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				BIOS, I/O Port & K/B CONN/TP CONN/PBTN			
				Document Number			Rev
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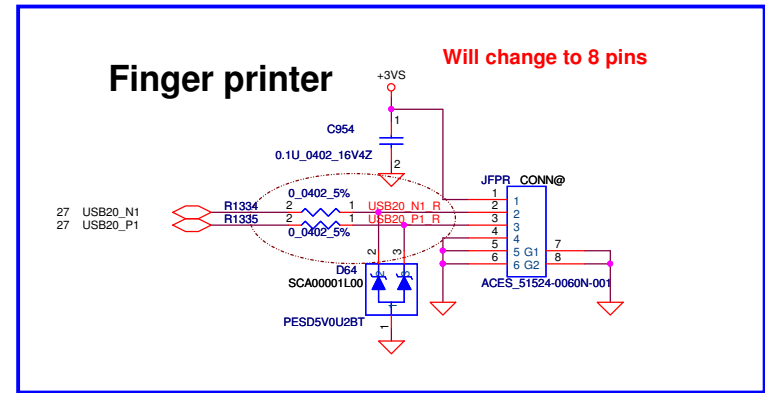
Keyboard backlight Conn



AOAC power control

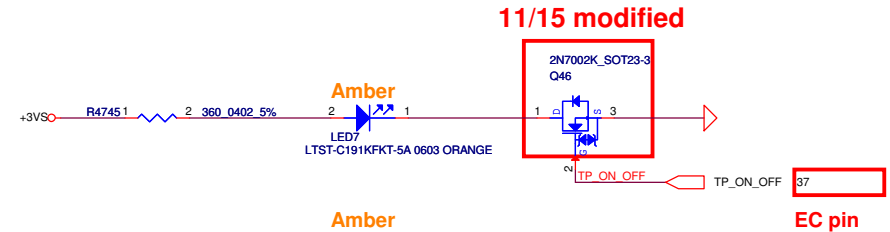
Del AOAC

WLAN ON/OFF LED



11/09 Change to KB connector

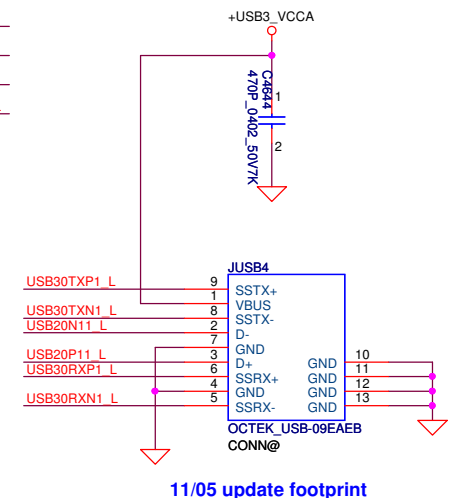
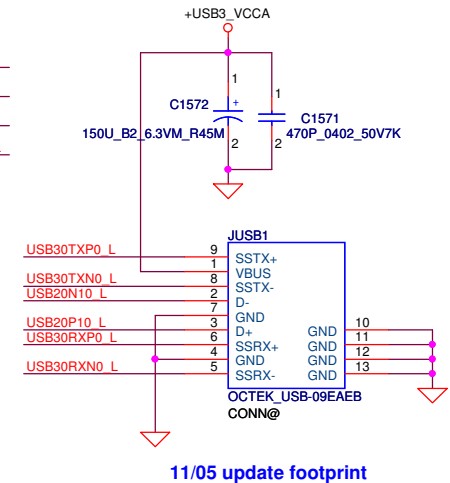
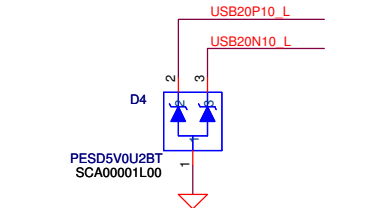
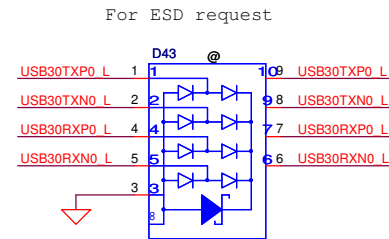
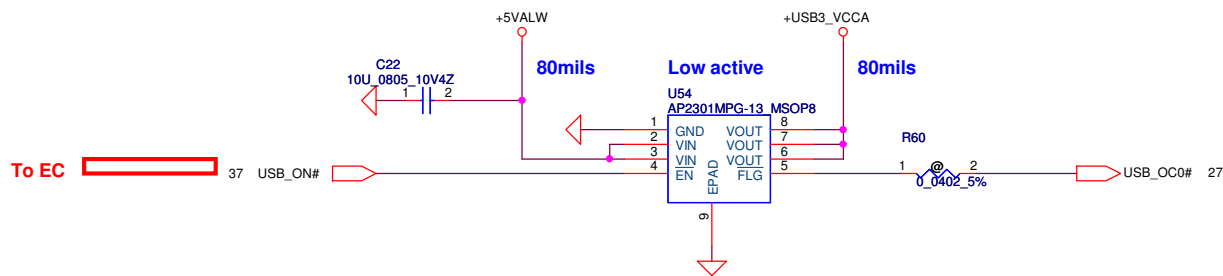
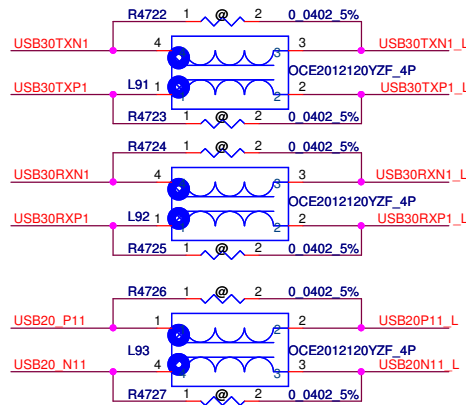
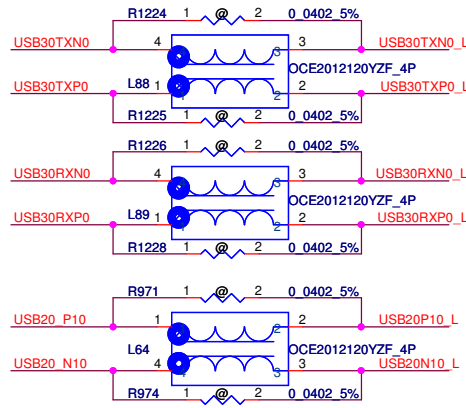
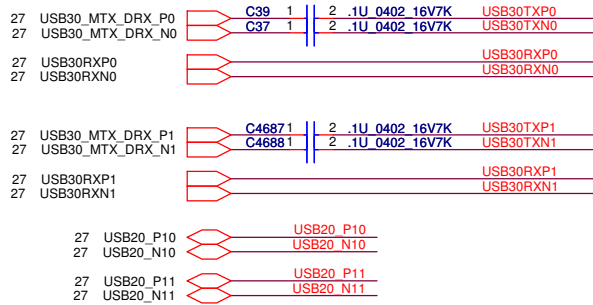
T/P On/Off LED



Mute On/Off LED

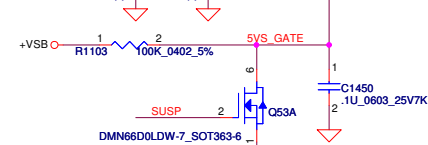
11/09 Change to KB connector

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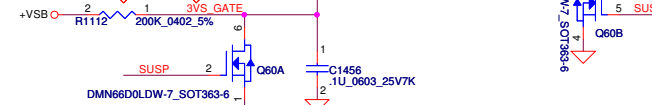


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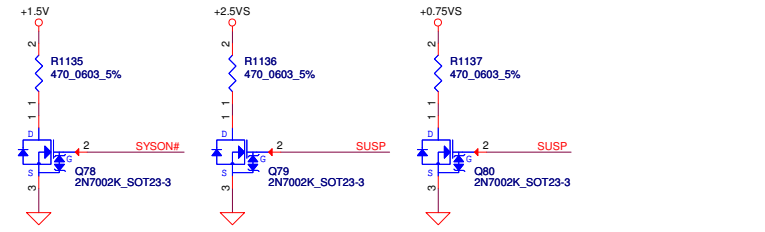
+5VALW TO +5VS (5A)



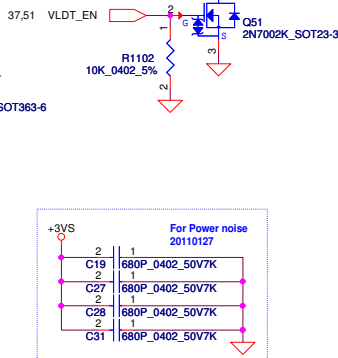
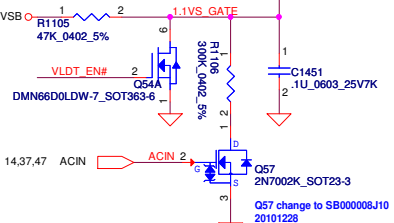
+3VALW TO +3VS (3.3A)



-1.5V TO +1.5VS (1.5A)



+1.1VALW TO +1.1VS (1.1A)

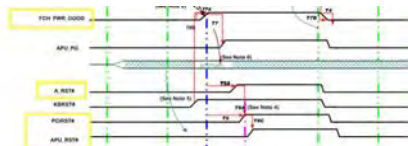
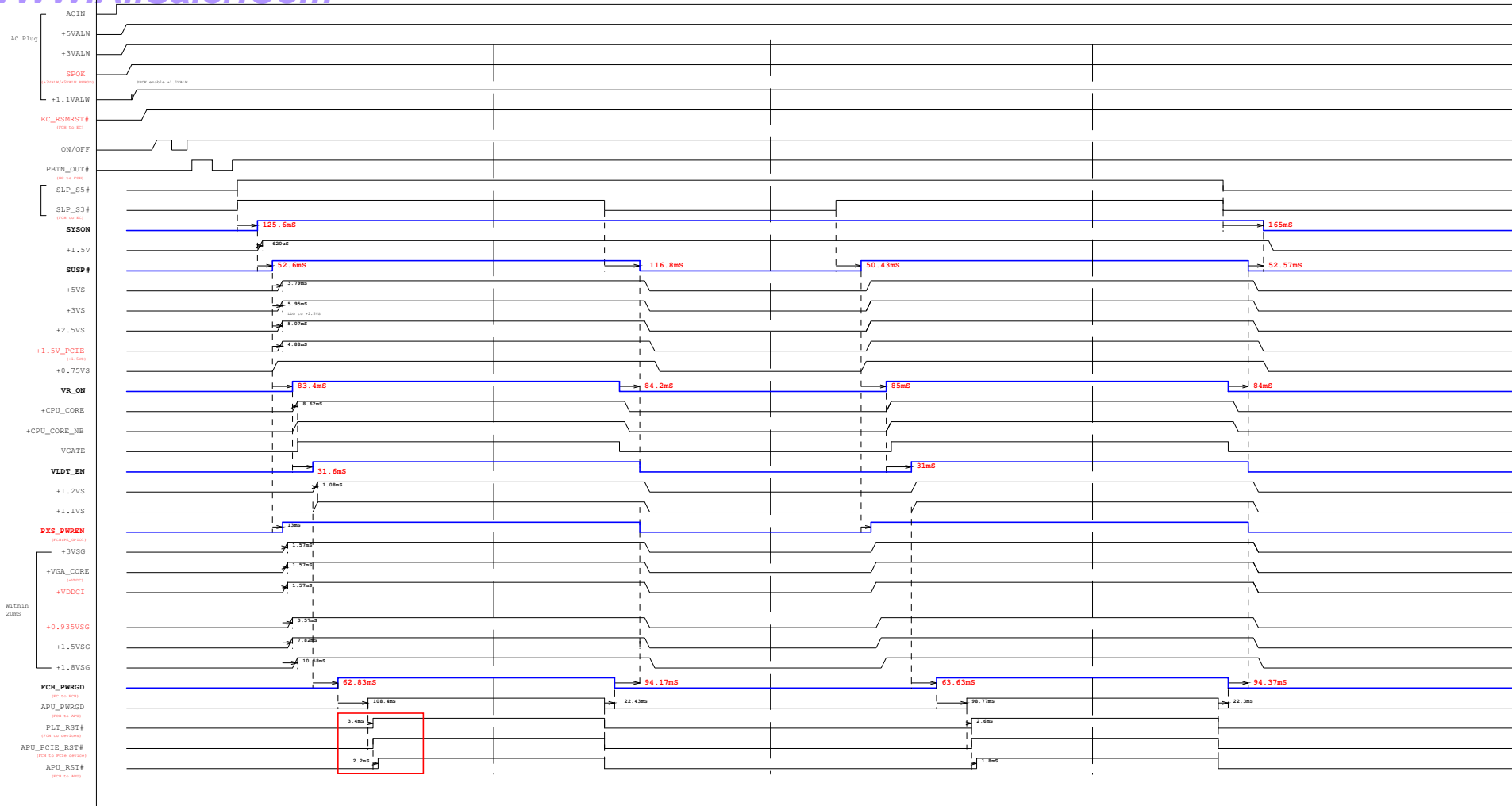


VGA Power

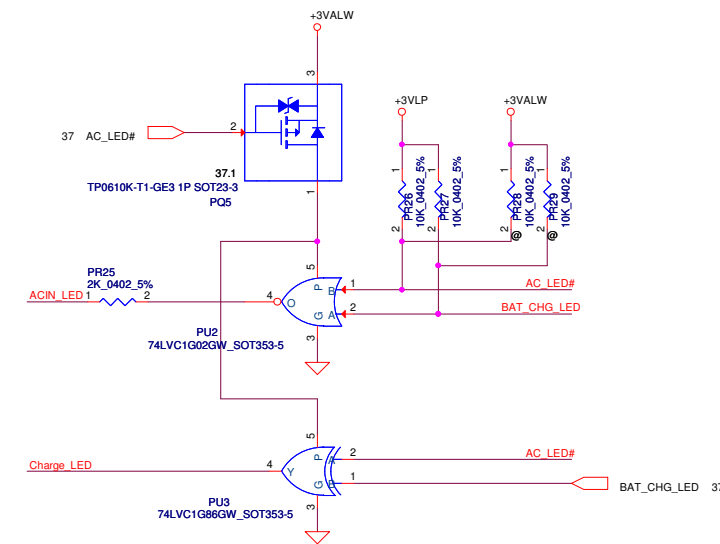
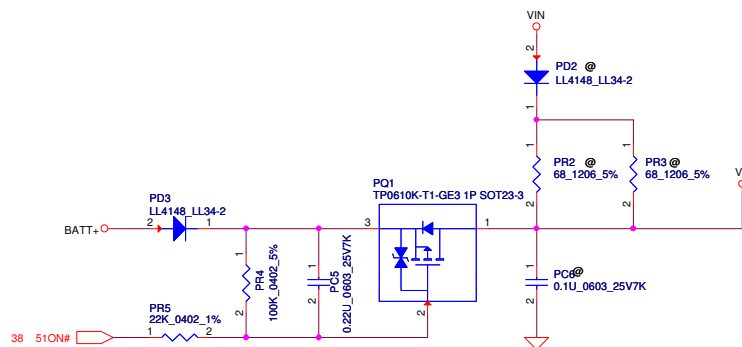
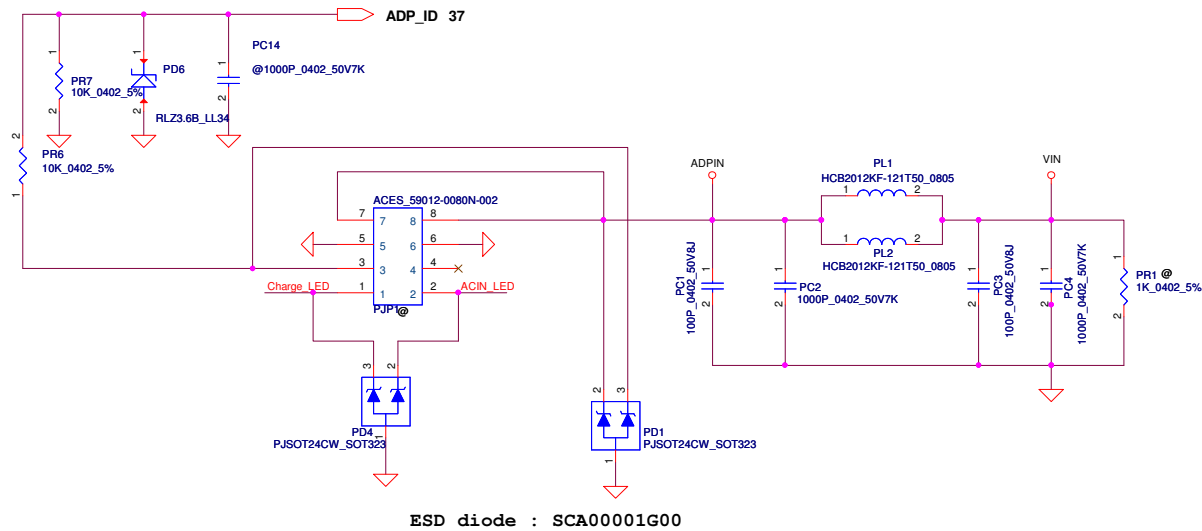
+1.5V to +1.5VSG (1.5A)

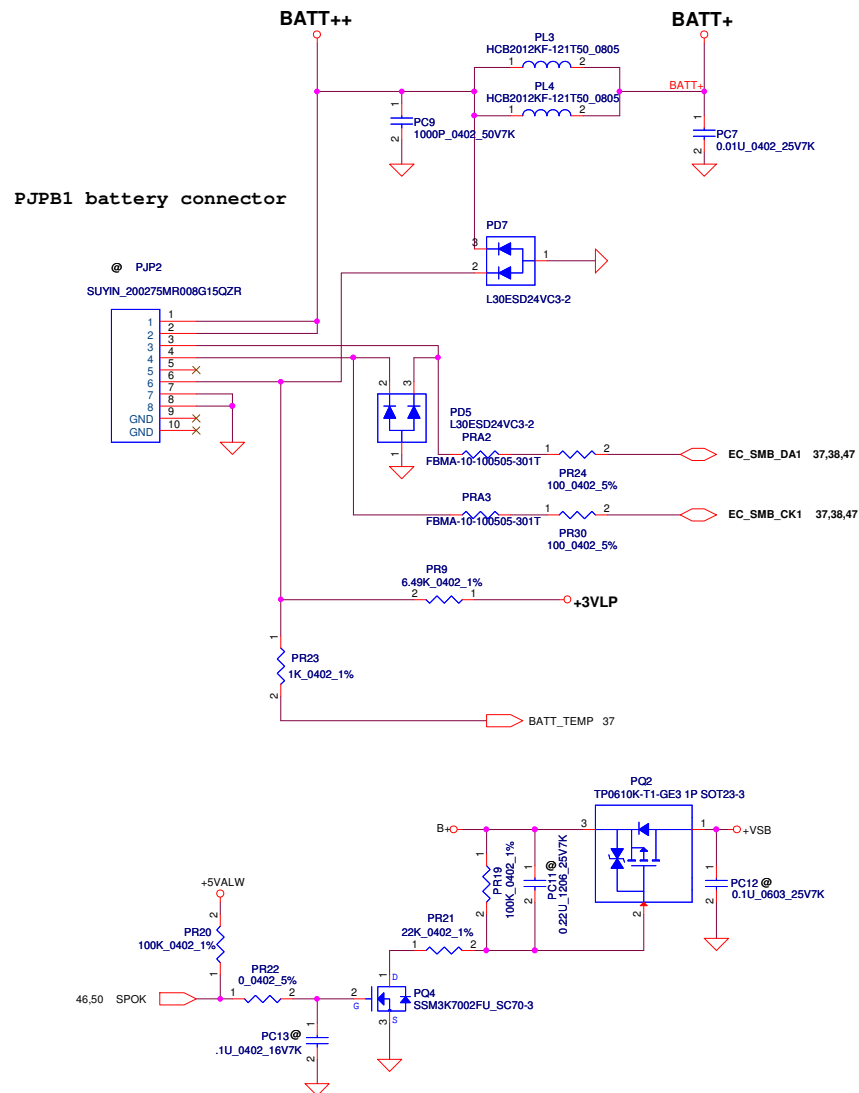
Del +1.5VSG and reserved on GPU

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				QCL51 LA-8712P		
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OCL51 LA-8712P		Rev		Rev	
Rev		Rev		Rev	

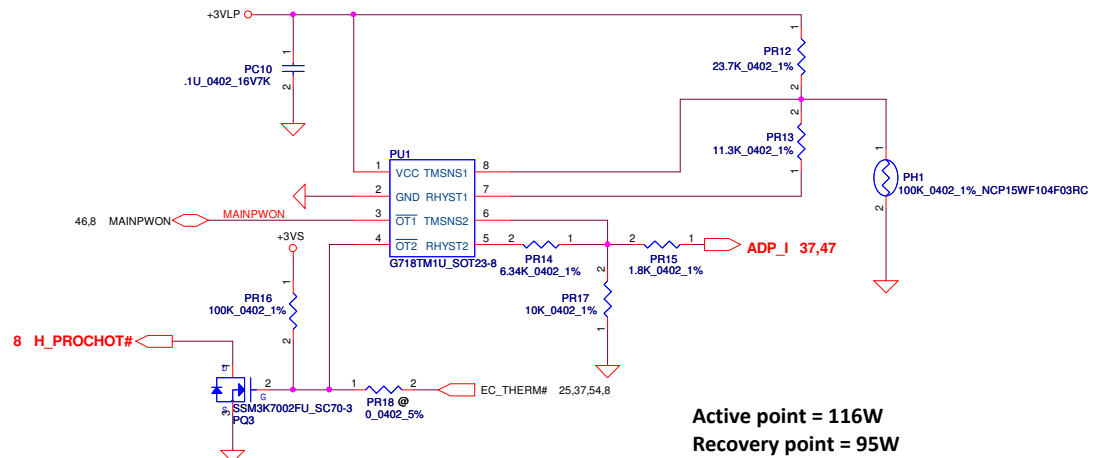




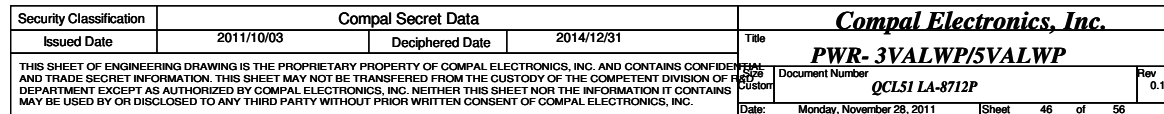
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

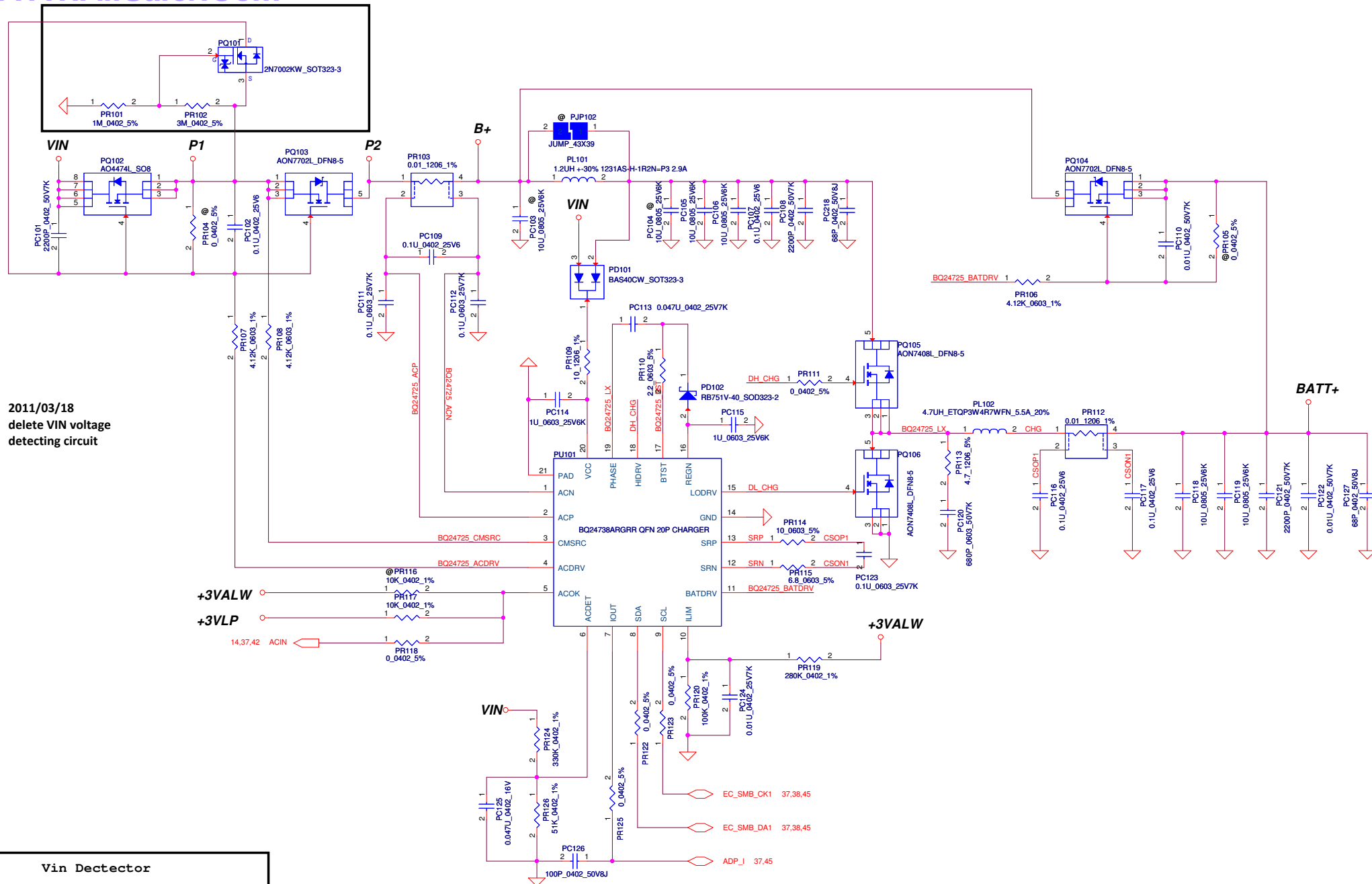
PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 56 +-3 degree C

$R_{set} = 3 * R_{tmh}$
 $R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$
 $R_{tmh} \text{ at } 90C = 7.8K, R_{tml} \text{ at } 56C = 26.1K$
 $R_{set} = 3 * 7.8K = 23.4K \Rightarrow 23.7K$
 $R_{hyst} = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \Rightarrow 11.3K$



Active point = 116W
Recovery point = 95W





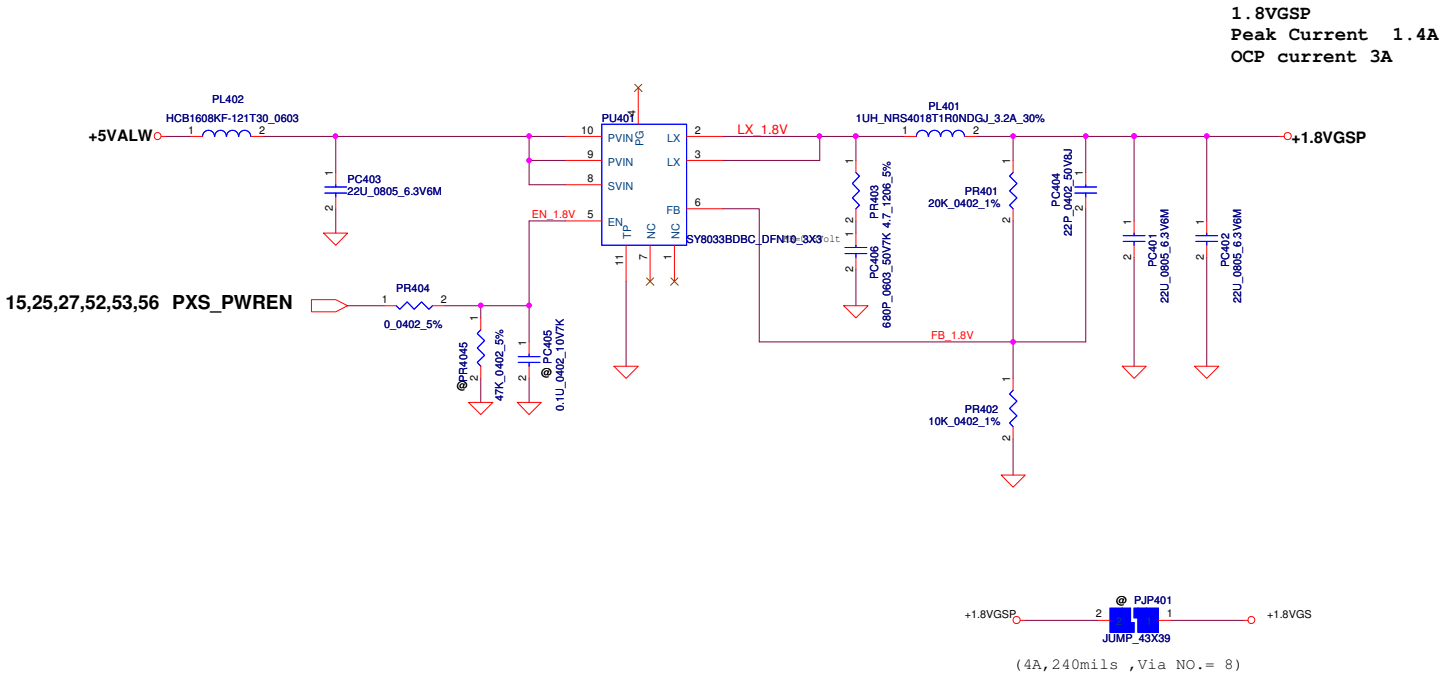
2011/03/18
delete VIN voltage
detecting circuit

Vin Detector

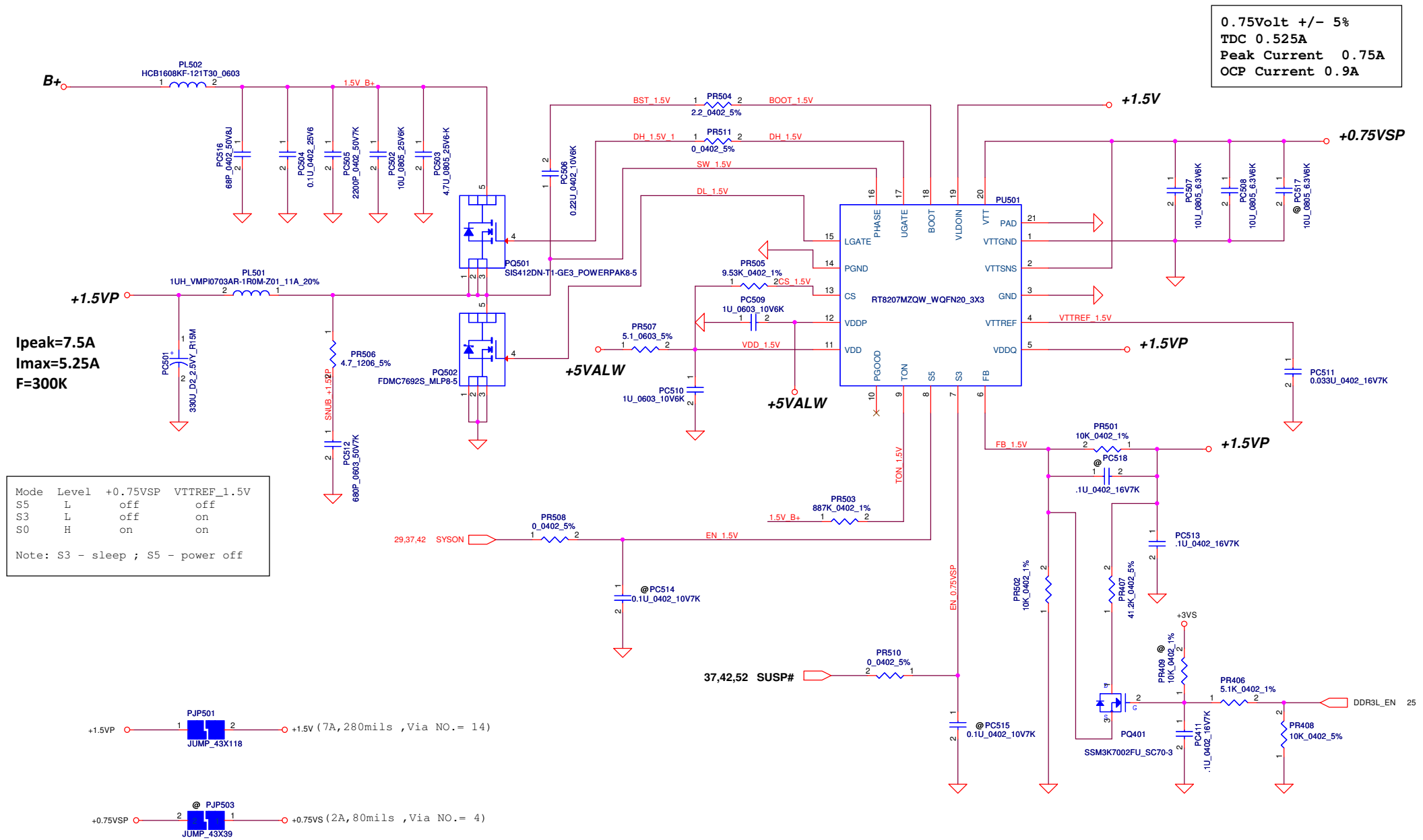
	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

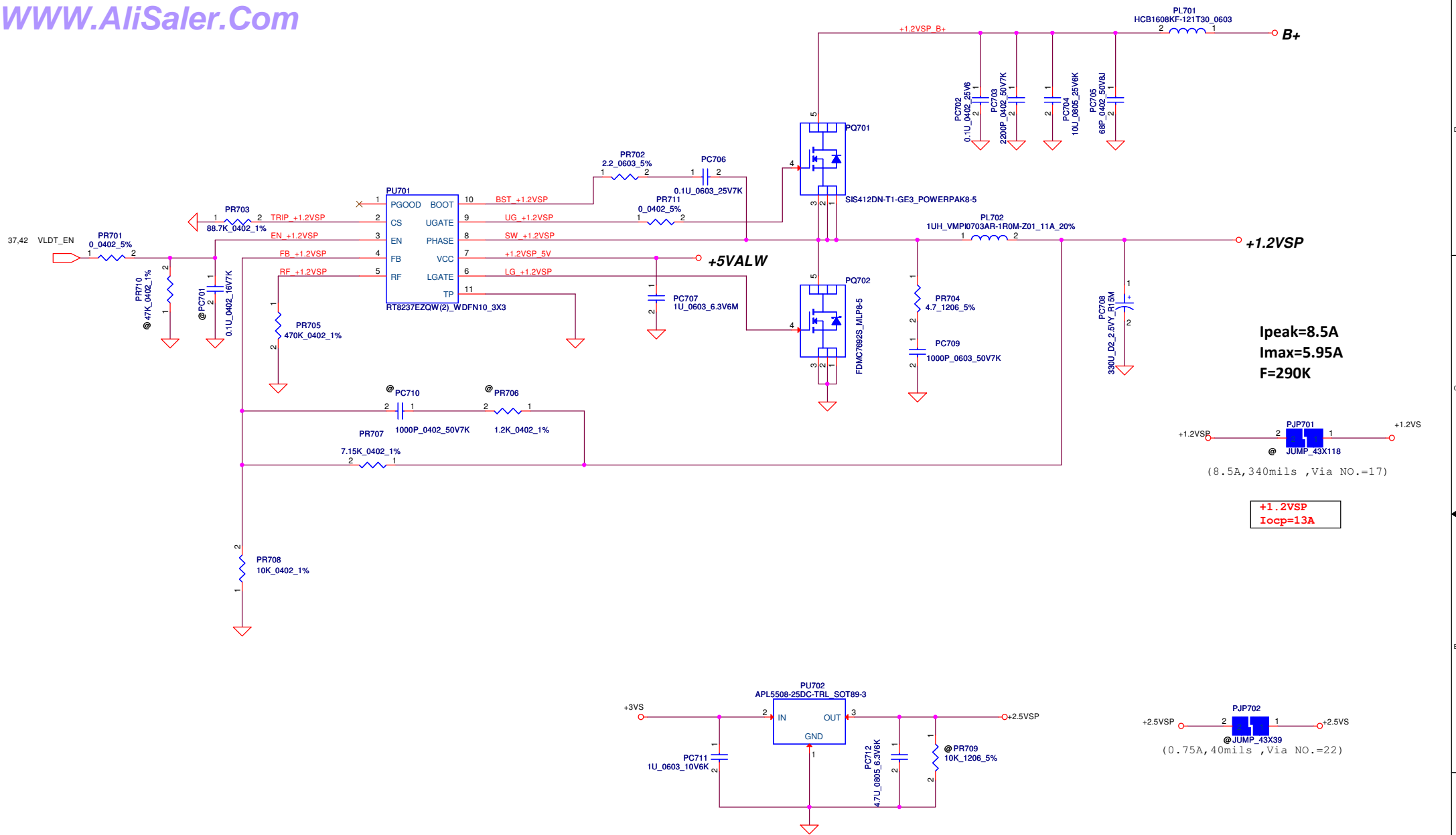
ILIM and external DPM
4.36A

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				Sheet	47 of 56
				Rev	0.1



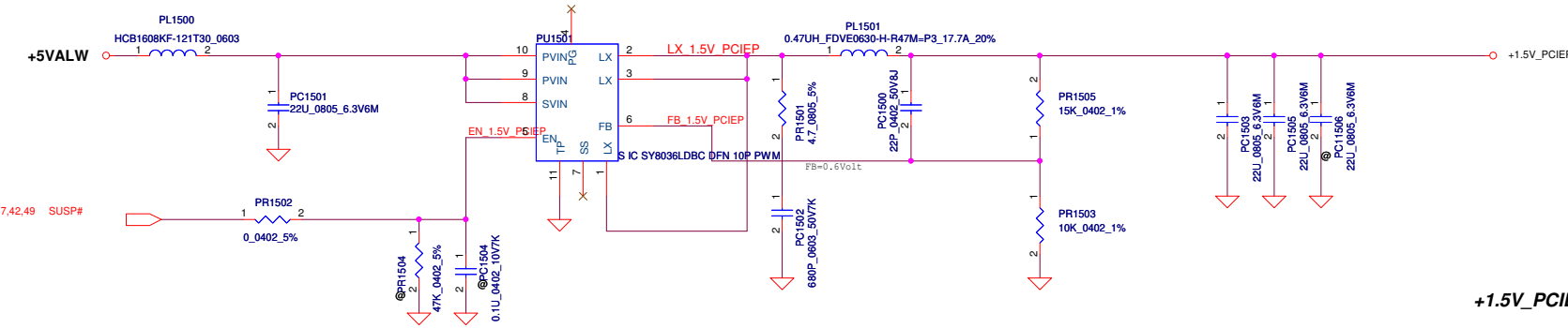
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						Size	Document Number
				LA-8712P		0.1	
Date:		Monday, November 28, 2011		Sheet		51 of 56	

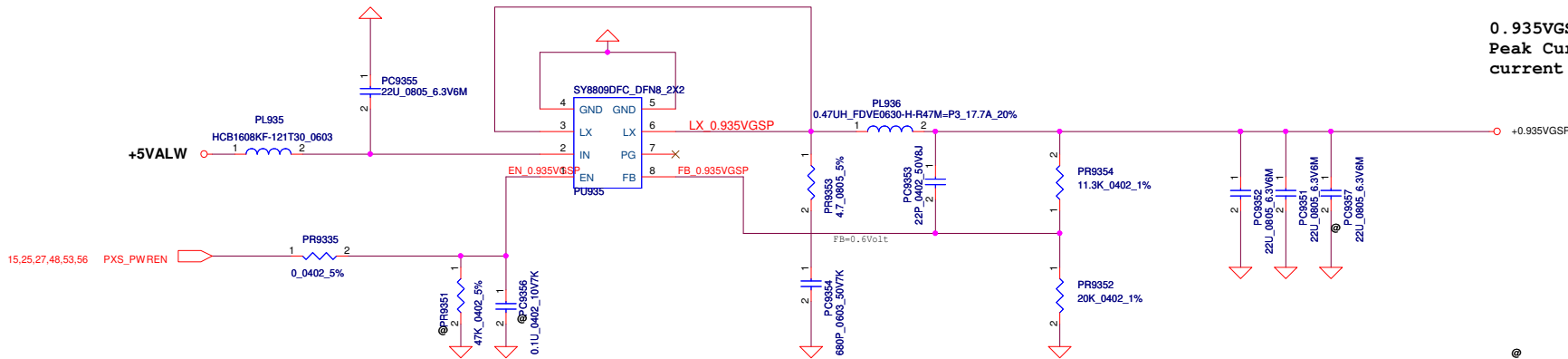
1.5VPCIEP
Peak Current 6A
OCP current 6A



+1.5V_PCIEP @ PJ1502 2 +1.5V_PCIE
JUMP_43X118

(6A, 240mils, Via NO.= 12)

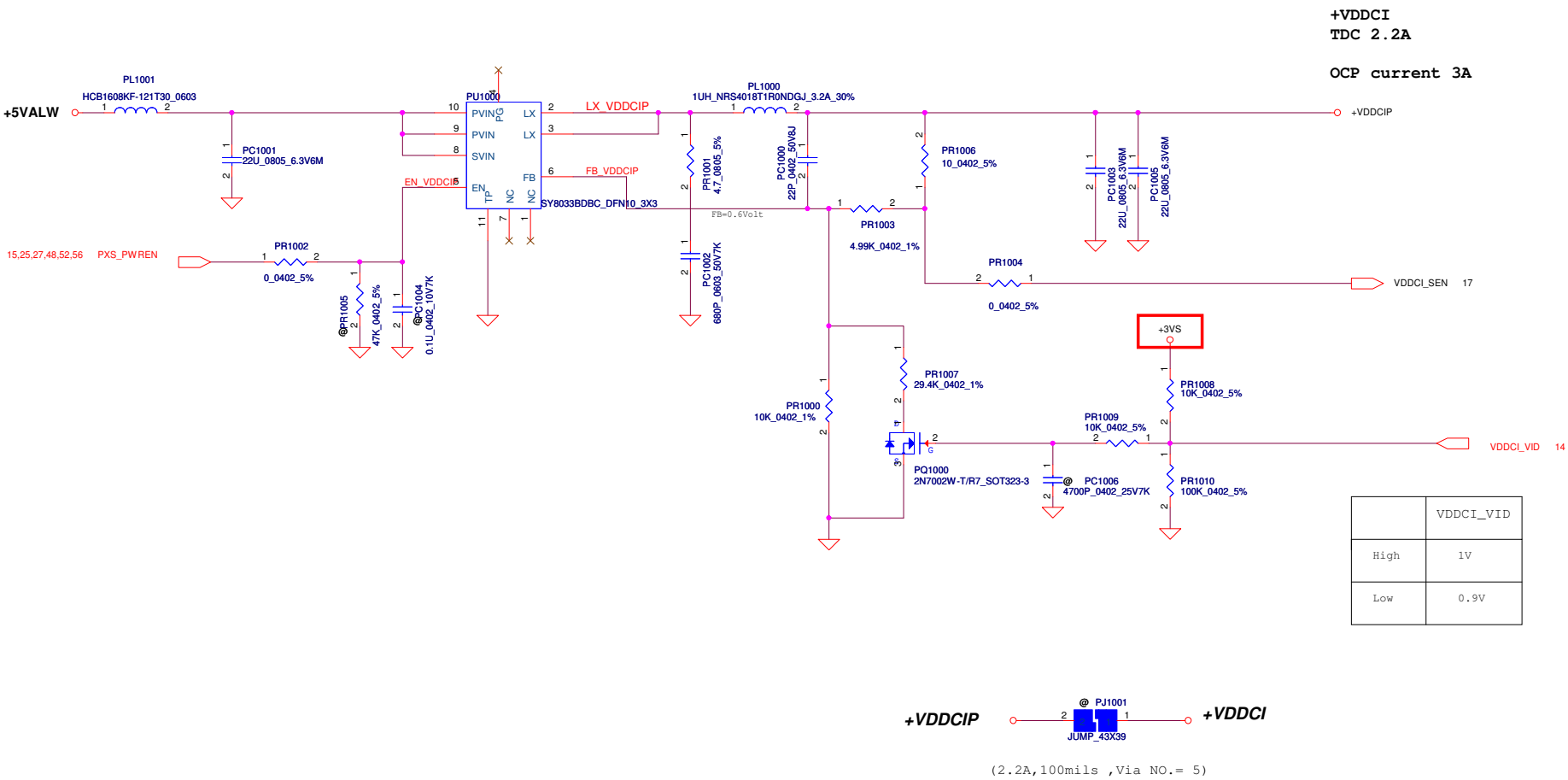
0.935VGSP
Peak Current 4.2A
current limited 6A

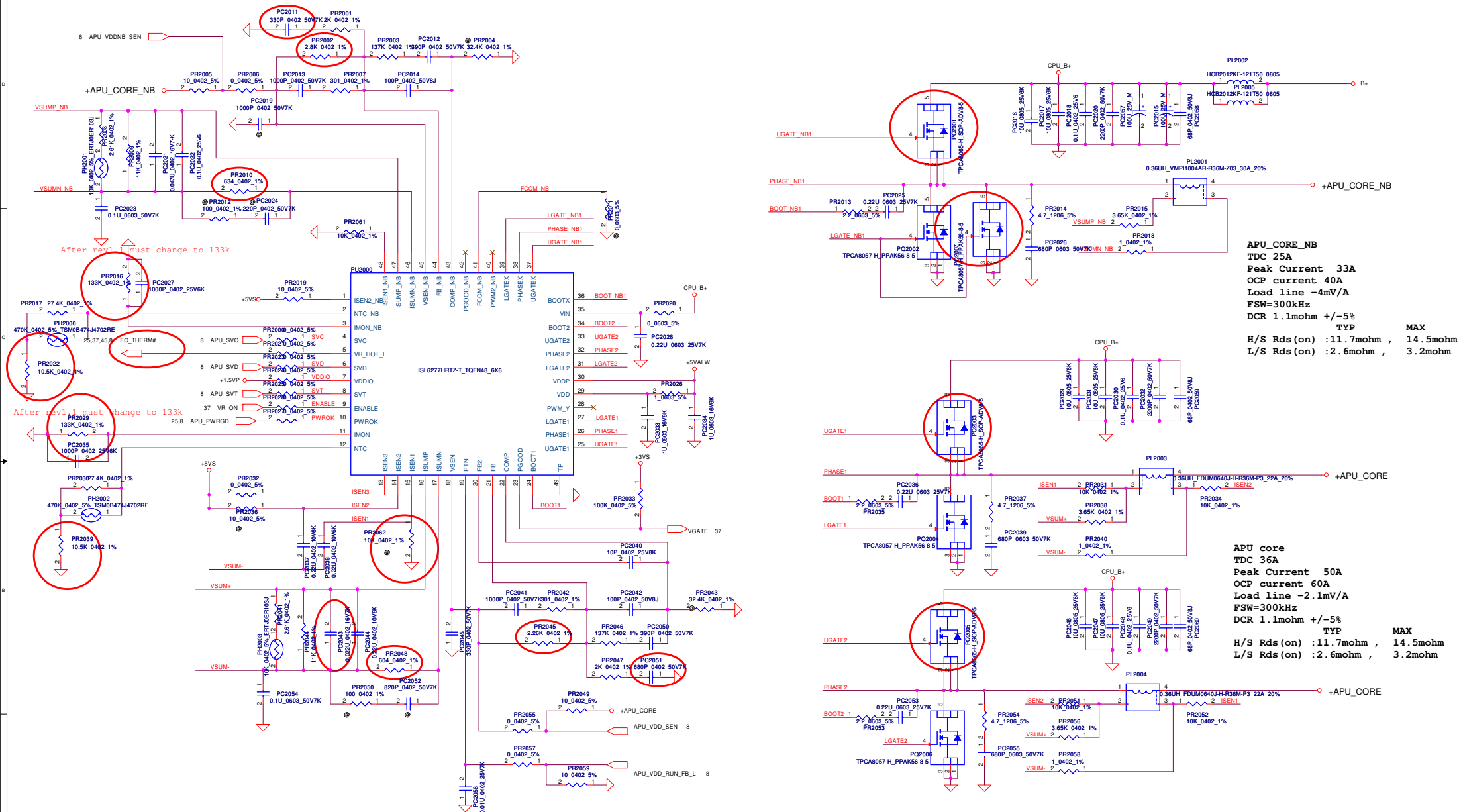


+0.935VGSP @ PJ9352 2 +0.935VGS
JUMP_43X118

(4.2A, 460mils, Via NO.= 8.4)

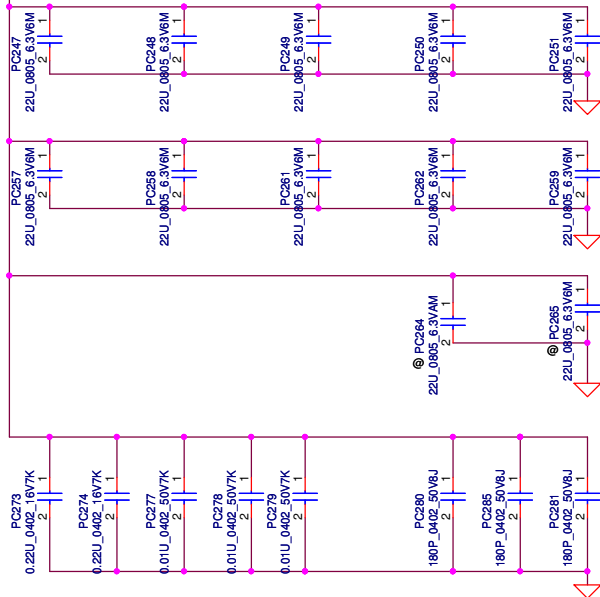
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Issued Date	2011/08/16	Deciphered Date	2012/08/15	Title	
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Date:	Monday, November 28, 2011	Sheet	52	of	56





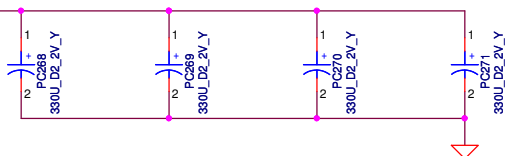
+APU_CORE

+APU_CORE



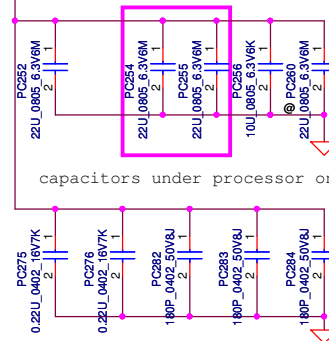
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Local



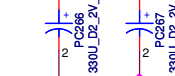
+APU_CORE_NB

+APU_CORE_NB



+APU_CORE_NB

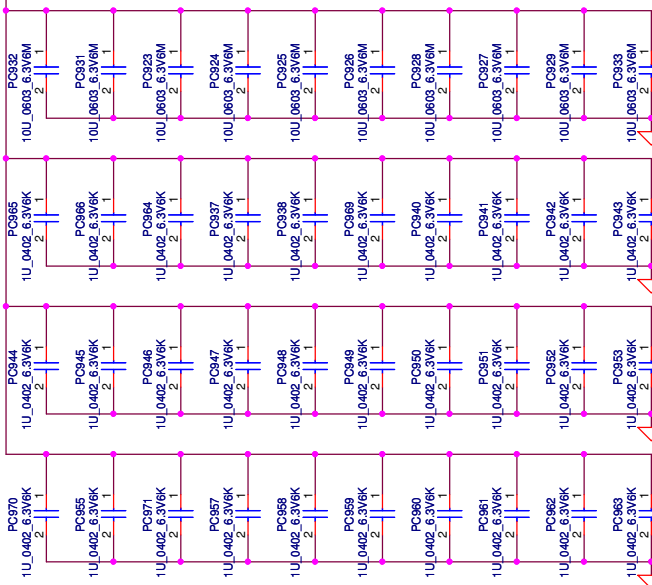
Local



+VGA_CORE

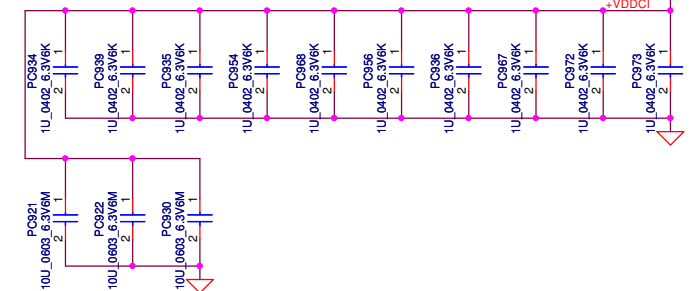
+VGA_CORE

+VDDC



+VDDCI

+VDDCI



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